SYLLABUS

1. Information about the program

1.1 Higher education institution	Universitatea Politehnica Timișoara
1.2 Faculty[1] / Department[2]	ELECTRONICS, TELECOMUNICATON AND INFORMATION TECHNOLOGIES/ Applied Electronics
1.3 Field of study (name/code[3])	ELECTRONIC ENGINEERING, TELECOMUNICATION AND INFORMATION TECHNOLOGIES / 20/20/10
1.4 Study cycle	Master
1.5 Study program (name/code/qualification)	Automotive Electronic Systems /20/20/10 / 2152

2. Information about discipline

2.1a Name of discipline/The educational classe[4]	High Performance Computing, Memories and Smart Sensors						
2.1b Name of discipline in Romanian							
2.2 Coordinator (holder) of course activities	Jivet Ioan						
2.3 Coordinator (holder) of applied activities[5]	Elisei-Stefan Ilies						
2.4 Year of study[6]	1	**2.5** Semester	1	**2.6** Type of evaluation	E	**2.7** Regime of discipline[7]	DOB

3. Total estimated time (direct activities (fully assisted), partially assisted activities and unassisted activities[8])

3.1 Number of hours fully assisted/week	4 ,of which:	course	2	seminar/laboratory/project		2
3.1* Total number of hours fully assisted/sem.	56 ,of which:	course	28	seminar/laboratory/project		28
3.2 Number of on-line hours fully assisted/sem	0 ,of which:	course	0	seminar/laboratory/project		0
3.3 Number of hours partially assisted/week	,of which:	project, research		training	hours designing M.A. dissertation	
3.3* Number of hours partially assisted/ semester	,of which:	project of research		training	hours designing M.A. dissertation	
3.4 Number of hours of unassisted activities/ week	4.93 ,of which:	Additional documentation in the library, on specialized electronic platforms, and on the field				1.5
		Study using a manual, course materials, bibliography and lecture notes				1.5
		Preparation of seminars/ laboratories, homework, assignments, portfolios, and essays				1.93
3.4* Total number of hours of unasssited asctivities/ semester	69 ,of which:	Additional documentation in the library, on specialized electronic platforms, and on the field				21
		Study using a manual, course materials, bibliography and lecture notes				21
		Preparation of seminars/ laboratories, homework, assignments, portfolios, and essays				27
3.5 Total hrs./week[9]	8.93					
3.5* Total hrs./semester	125					
3.6 No. of credits	5					

4. Prerequisites (where applicable)

4.1 Curriculum	• Basics of Microprocessors and Memories
4.2 Learning outcomes	• -

5. Conditions (where applicable)

5.1 of the course	• Video-projector, Internet connection
5.2 to conduct practical activities	• PC's with Software Tools, Electronic Basic Tools

6. Learning outcomes acquired through this discipline

Knowledge	C1. The student/graduate demonstrates advanced knowledge of the categories of electronics, the principles of electricity and engineering, and the physics and mathematics required for the design and analysis of complex electronic systems. C9. The student/graduate demonstrates advanced knowledge of the operating principles and integration of microsystems and MEMS. C16. The student/graduate demonstrates advanced knowledge of the operating principles, typologies, and applications of sensors. •
Skills	• A3. The student/graduate designs electronic systems, including circuits, equipment, and applications in fields such as automotive and instrumentation A6. The student/graduate applies testing and validation procedures for electronic products, systems, and components. A23. The student/graduate designs sensors, selecting appropriate materials and technologies for specific applications. •
Responsibility and autonomy	RA1. The student/graduate assumes responsibility for coordinating and approving engineering projects, assessing the technical, economic, and environmental impact of proposed solutions. RA2. The student/graduate demonstrates autonomy in leading scientific research and making complex engineering decisions, coordinating multidisciplinary technical teams. RA17. The student/graduate assumes responsibility for the quality and functionality of designed and tested sensors. •

7. Objectives of the discipline (based on the grid of learning outcomes acquired)

- Understand the concepts behind high performance computing architectures required for the processing of the high volume of data in intelligent systems. Understand the concepts for data protection in complex architecture that ensure the safety requirements for automotive software design
- Good understanding of high performance computing cores. Good understanding of Multi-processor system and on-chip communication infrastructure. Good understanding of memory organization and protection. Good understanding of GPUs and data parallel processing.

8. Content

8.1 Course	Number of hours	Of which online	Teaching methods
L1. Microprocessor Architecture from Embedded to HPC	2	0	Theoretical presentation with questions and discussions, correlating concepts with real-world applications.
L2. RISC V ISA basics - principles of RISC Architecture	2	0	
L3. Memory Models - definition of VM, Cashe Memory, Physical memory	2	0	
L4. Paging memory for RISC V , TLB and Privilage levels	2	0	
L5. Cache Memory basics and replacement policies	2	0	
L6. Privilaged levels of RISC V and CSc's registers	2	0	
L7. Pipelined architecture as a Option of RISC V systems for HPC	2	0	

L8. Multiple Core processors and Cache Distributed Coherency	2	0	
L9. RISC V Interupts, Exceptions and Traps	2	0	
L10 Examples of RISC V SOC - Sifive ecosystem L11 Examples of RISC V SOC - Sifive ecosystem	2 2	0	
L12 Advanced Topics in HPC L13 Advanced Topics in HPC L14 Advanced Topics in HPC	2 2 2	0	

	Bibliography[10] Online Cource: Technische Univrsitat Berlin. Prof. Dr. Ben Juulink High-Performance and Embedded Computer Architectures. Computer Organization and Design: The Hardware/Software Interface, David A. Patterson și John L. Hennessy Computer Architecture: A Quantitative Approach, John L. Hennessy și David A. Patterson

8.2 Applied activities[11]	Number of hours	Of which online	Teaching methods
Lab1. Exploring the documentation and codes for RV Implementations: SweRV master, NeoRV on Github	2		Hands-on experimenting on programing, FPGA Implementation
Lab2. C Programming Lab3 RISC-V Assembly Language Programming	2 2		
Lab 4 Function Calls	2		
Lab5 Introduction to I/O programming	2		
Lab 6. RVfpga Timers and programming	2		
Lab 7. Pipeline Microprocessors Lab 8. Pipeline Microprocessors	2 2		
Lab9. RISC V – experience with ESP32C3 boards Lab10. RISC V – experience with ESP32C3 boards	2 2		
Lab 11. Special topics to experiment on RISC V – Github Online Codes: Leaf, Lab 12. Special topics to experiment on RISC V – Github Online Codes: NeoRV32 Lab 13. Special topics to experiment on RISC V – Github Online Codes: Ibex Lab 14. Special topics to experiment on RISC V – Github Online Codes: OpenTitan	2 2 2 2		

	Bibliography[12] Online Courese on RISC V: Imagination Techonoly, 2024, Online RISC V Documentation Computer Organization and Design: The Hardware/Software Interface, David A. Patterson și John L. Hennessy Computer Architecture: A Quantitative Approach, John L. Hennessy și David A. Patterson

9. Evaluation

Type of activity	**9.1** Evaluation criteria[13]	**9.2** Evaluation methods	**9.3** Share of the final grade

9.4 Course	Verification of theoretical knowledge about HPC architectures (RISC-V, ARM), memory, data protection, and multiprocessor systems. Explanation of concepts and relationships between architecture components (ISA, cache memory, TLB, privilege levels).	Writter Test	66%
9.5 Applied activities	**S:**		
	L: Solving problems or exercises involving memory organization, cache coherence, interrupts, and exceptions.	Q&A	34%
	P:		
	Pr:		
	Tc-R[14]:		
9.6 Minimum performance standard (minimum amount of knowledge necessary to pass the discipline and the way in which this knowledge is verified[15]			
• The student must demonstrate understanding of the fundamental concepts of RISC-V architecture and memory organization (ISA, cache memory, TLB, privilege levels).			

Date of completion	**Course coordinator (signature)**	**Coordinator of applied activities (signature)**
24.09.2025		
Head of Department (signature)	**Date of approval in the Faculty Council** [16]	**Dean (signature)**
	7.10.2025	