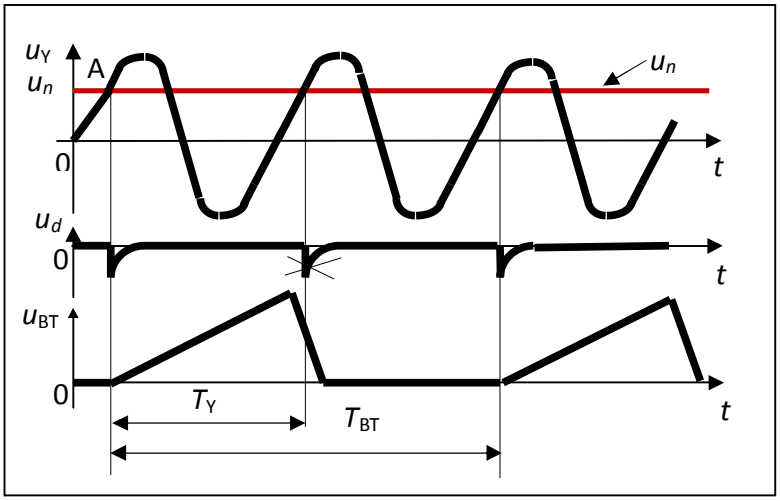
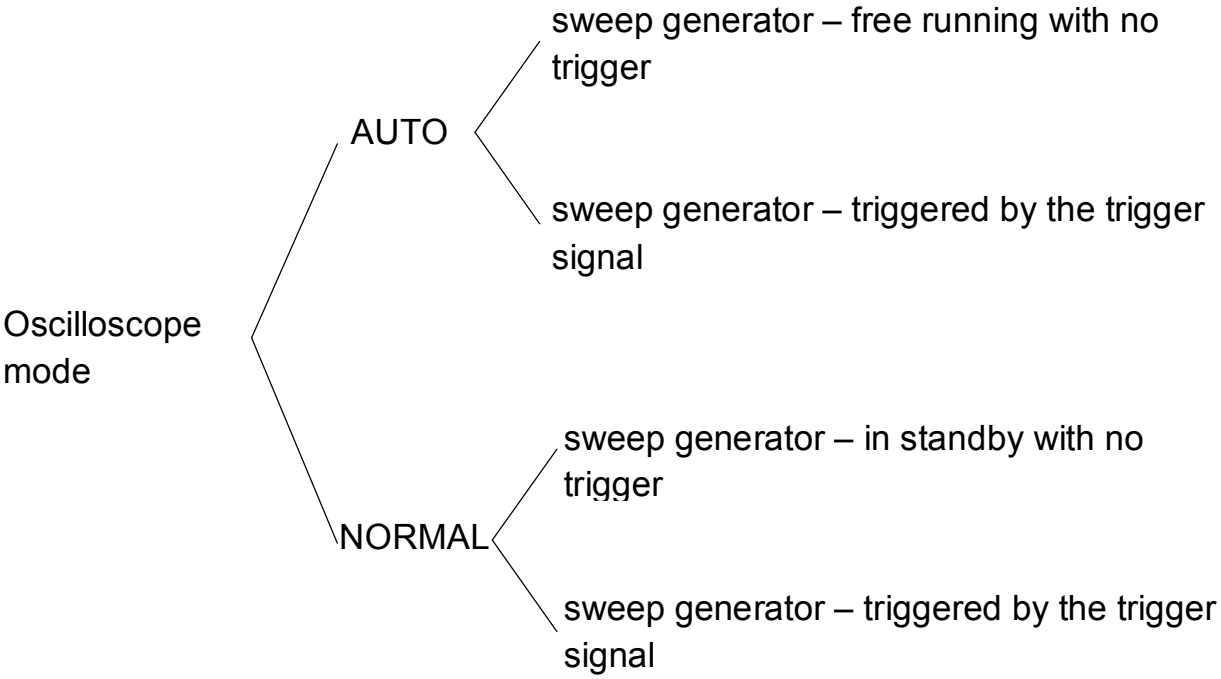
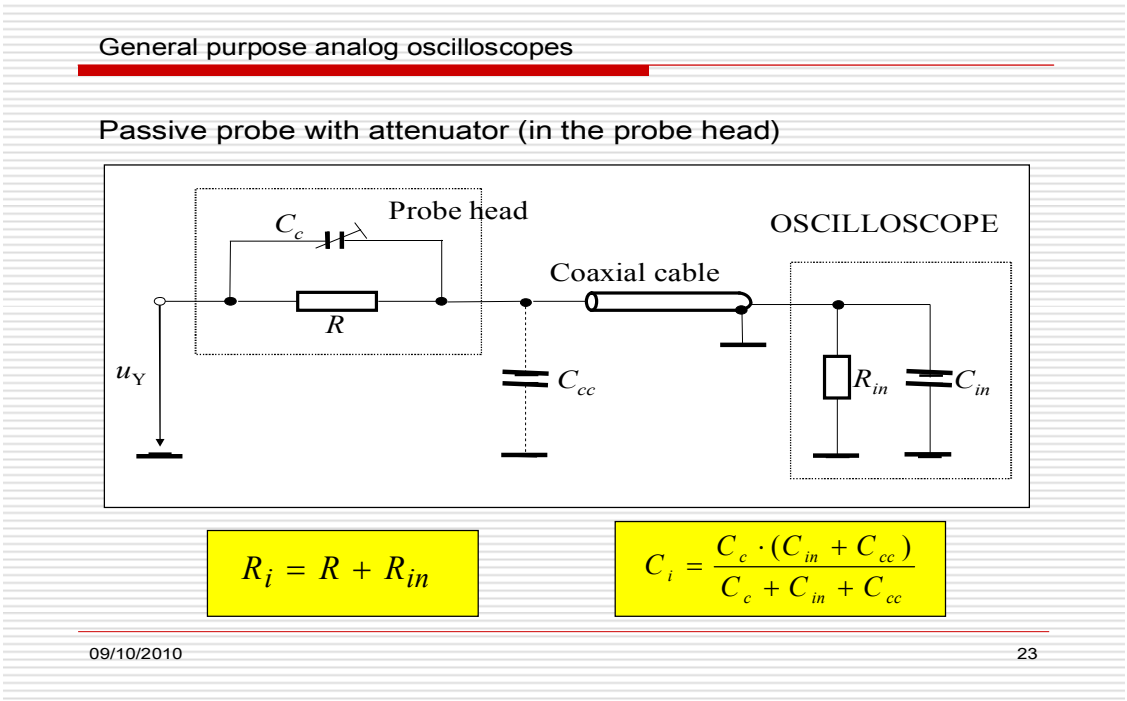




3. ***Probes for oscilloscopes. Attenuating probes. Frequency compensation. Describe what happens and tell (and draw) how the image of square pulses appears on the screen when the compensation condition is not met.***

https://intranet.etc.upt.ro/~E_INSTR/PowerPoint%20presentations%202010%202011/1%20Oscilloscopes%202010%202011.ppt, slides #23-25



Probes without and with attenuator - comparison

Probe without attenuator

- advantage – it does not attenuate the input signal
- disadvantage – relatively small input resistance (1 MΩ), large input capacitance (50 - 150 pF)

Probe with attenuator

- advantage – large input resistance (10 MΩ), small input capacitance (5 - 15 pF)
- disadvantage – it attenuates the input signal (therefore, the value read on the display must be multiplied by the probe's attenuation factor)

4. *General purpose analog oscilloscopes. Delayed sweep: use, operating modes, utility.*

https://intranet.etc.upt.ro/~E_INSTR/PowerPoint%20presentations%202010%202011/1%20Oscilloscopes%202010%202011.ppt, slides #48-50

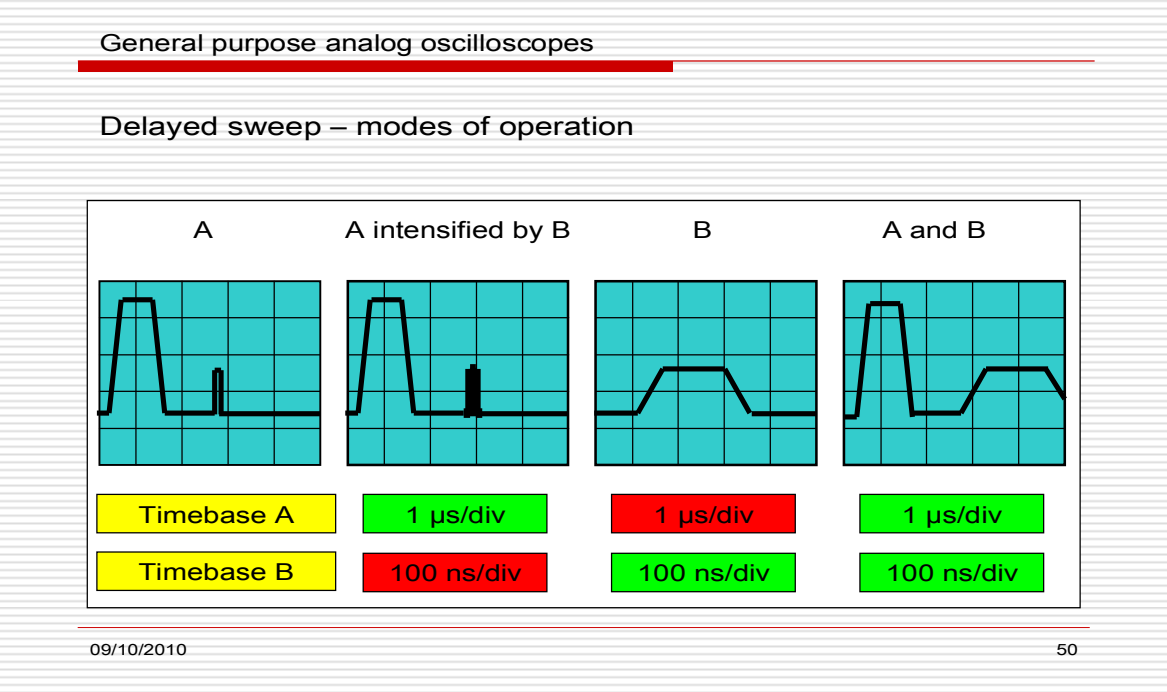
Delayed sweep

- found on more-sophisticated oscilloscopes, which contain a second set of timebase circuits for a delayed sweep.
- provides a very-detailed look at some small selected portion of the main timebase.

The main timebase serves as a controllable delay, after which the delayed timebase starts. This can start when the delay expires, or can be triggered (only) after the delay expires. Ordinarily, the delayed timebase is set for a faster sweep, sometimes much faster, such as 1000:1. At extreme ratios, jitter in the delays on consecutive main sweeps degrades the display, but delayed-sweep triggers can overcome that.

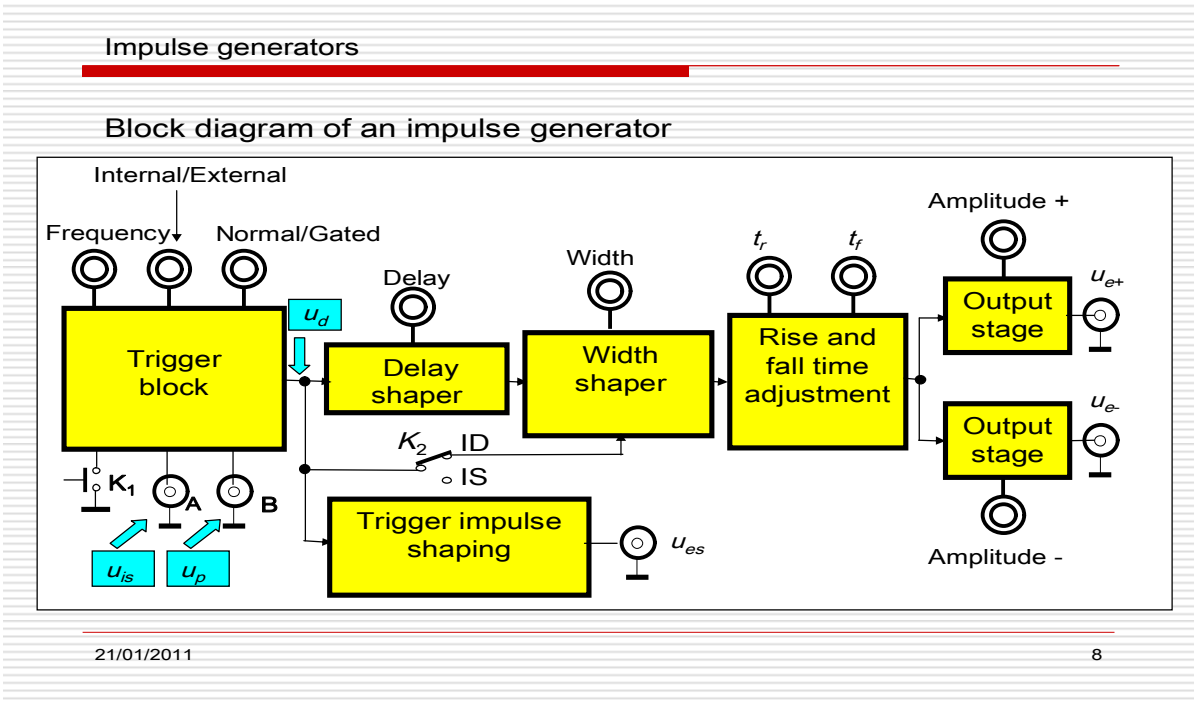
Operating modes

- A
- A intensified by B
- B
- A and B (mixed)



5. *Signal generators. Describe the operation of the pulse generator in single and double pulses modes.*

https://intranet.etc.upt.ro/~E_INSTR/PowerPoint%20presentations%202010%202011/2%20Signal%20Generators%202010%202011.ppt, slides #8-11



Operating modes

1. NORMAL

- ❑ internally triggered (simple or double impulses)
- ❑ externally triggered (simple or double impulses)
- ❑ single impulses (simple or double impulses)

2. GATED

- ❑ simple or double impulses

Operating modes

Normal, internally triggered, simple positive impulses

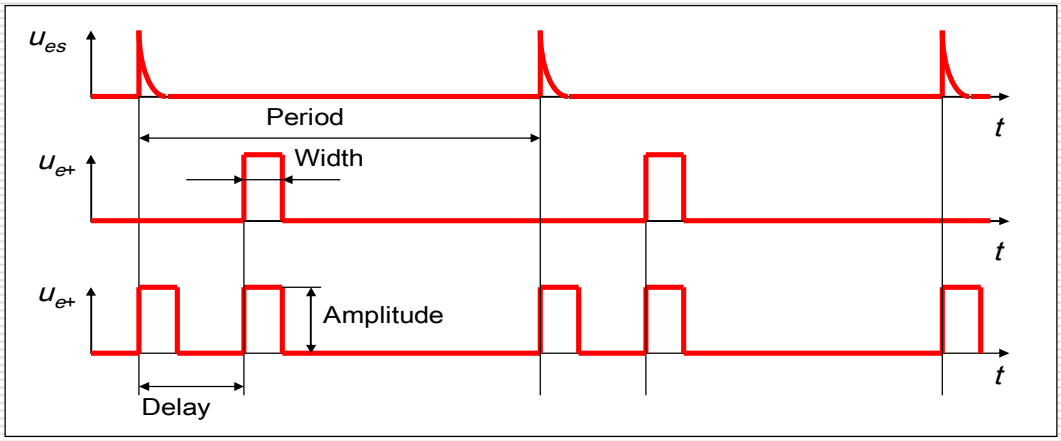
The trigger block operates autonomously and sets the repetition rate of the generated impulses.

The generator provides, in each cycle, a trigger pulse and one pulse at each output (positive and negative), delayed with respect to the trigger pulse.

Impulse generators

Operating modes

Normal, internally (or externally) triggered, simple or double positive impulses



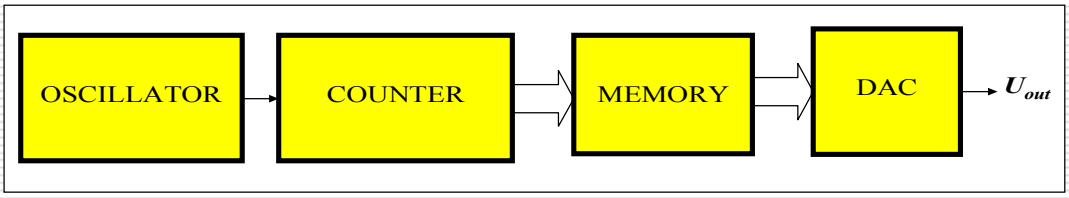
21/01/2011 11

6. *Signal generators. Describe the operation principle of a Direct Digital Synthesis generator.*

https://intranet.etc.upt.ro/~E_INSTR/PowerPoint%20presentations%202010%202011/2%20Signal%20Generators%202010%202011.ppt, slides #35-36

Sine wave generators

Direct digital synthesis generators

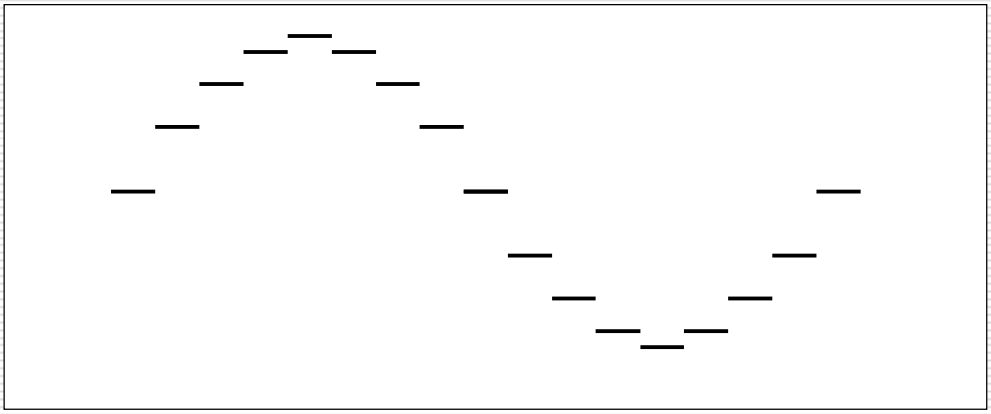


Oscillator (clock generator) – frequency f_0
Counter – n bits (0 - 2^n-1) = memory address
Stored values: $\sin(2\pi i/2^n)$
Output frequency: $f_0/2^n$

21/01/2011 35

Sine wave generators

Direct digital synthesis generators - example (n=4)



21/01/2011 36

7. ***Digital voltmeters and multimeters. Specify the measurement result for a 100% confidence level (result ± uncertainty, confidence level) according to the rules for data presentation when measuring a voltage of 12.45 V with a 3 ½ digit 20 V voltmeter whose maximum permissible error is given by***

$$\Delta_t = 0{,}1\% \times \text{reading} + 0{,}05\% \times \text{range} + 1 \text{ digit}$$

https://intranet.etc.upt.ro/~E_INSTR/PowerPoint%20presentations%202010%202011/3%20Digital%20Voltmeters%20and%20Multimeters%202010%202011.ppt, slides #7-10

Introduction

The maximum permissible error

Δ_t=a% × reading + b% × range + n digits

Δ_t=a% × reading + c% × range

Δ_t=a% × reading + m digits

Remark. One digit represents one LSD.

Example. One digit is 1 mV in case of a 2 V, $3^1/_2$ digit DVM (readout x,xxx V).

21/01/2011 7

Introduction

Data presentation rules

1. Measurement error and uncertainty should be expressed with no more than two significant digits.
2. The LSD of the measurement result and of its corresponding error/uncertainty should have the same weight.

Examples.

Right	Wrong
0,2%	0,256%
3,5 mV	3,58 mV
0,02 mA	0,0222 mA

Right	Wrong
1,0 ± 0,2 mA	1 ± 0,2 mA
1,538 V ± 0,003 V	1,538 V ± 0,03 V
1,538 V ± 3 mV	1,53 V ± 3 mV

21/01/2011 8

Exercise. The maximum permissible error of a 20V, $3^{1/2}$ digit DVM is given by

$$\Delta t = 0{,}1\% \times \text{reading} + 0{,}05\% \times \text{range} + 1 \text{ digit}$$

Determine the uncertainty for a measured value of 12.45 V and specify the measurement result corresponding to a confidence level of 100%.

Present the other two forms of the maximum permissible error.

Solution. The DVM reads xx,xx V. Therefore,

1 digit = 10 mV.

The maximum permissible error when measuring 12.45 V is

$\Delta t = 0{,}1\% \times 12.45 \text{ V} + 0{,}05\% \times 20 \text{ V} + 10 \text{ mV}$,

or

$\Delta t = 32.45 \text{ mV} \cong 30 \text{ mV}$.

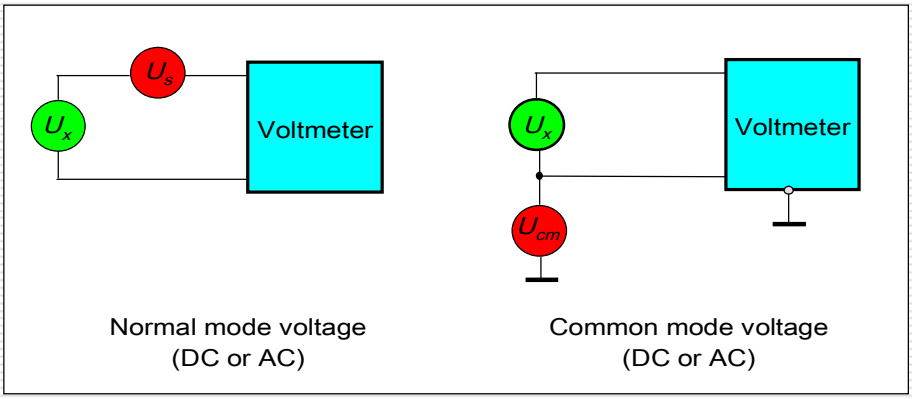
For a confidence level of 100%, the measurement result should be specified as

$U = 12.45 \text{ V} \pm 30 \text{ mV}$.

8. *Digital voltmeters and multimeters. Define normal and common mode voltages and the respective rejection ratios (NMRR and CMRR)*

https://intranet.etc.upt.ro/~E_INSTR/PowerPoint%20presentations%202010%202011/3%20Digital%20Voltmeters%20and%20Multimeters%202010%202011.ppt, slides #20, 23, 28

Measurement errors due to external noise



Normal mode voltage (DC or AC)

Common mode voltage (DC or AC)

The ability of a DC DVM to reject an AC normal mode signal is described by the Normal Mode Rejection Ratio (acronym NMRR):

$$NMRR = \frac{\text{amplitude of the normal mode voltage}}{\text{equivalent DC voltage}}$$

Example. For a DC DVM with a NMRR of 100, a normal mode voltage with an amplitude of 1 V produces an additional error of

1 V/100 = 0,01 V = 10 mV.

DC digital voltmeters

The ability of a DC DVM to reject a common mode signal is described by Common Mode Rejection Ratio (acronym CMRR):

$$CMRR = \frac{\text{tensiunea perturbato are de mod comun}}{\text{tensiunea serie echivalent ă}}$$

Aplicație. Un voltmetru de tensiune continuă are CMRR = 1000. O tensiune de mod comun de 5 V conduce la o tensiune serie echivalentă de 5 V/1000 = 5 mV.

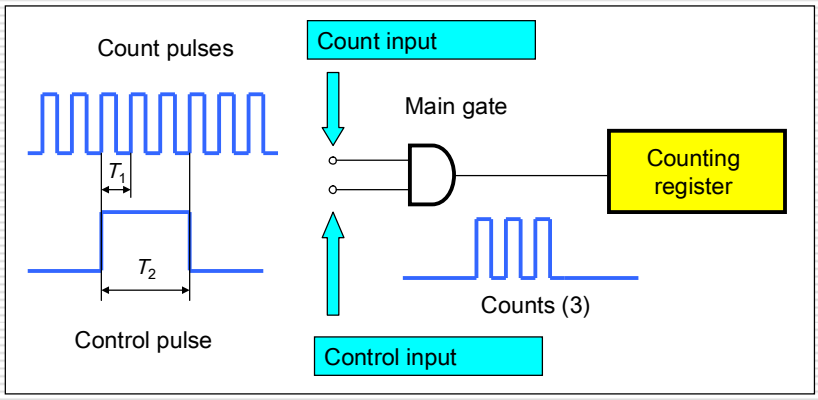
21/01/2011 28

9. *Universal counters. Describe the operating principle and explain how frequency can be measured.*

https://intranet.etc.upt.ro/~E_INSTR/PowerPoint%20presentations%202010%202011/4%20Universal%20counters%202010%202011.ppt, slides #6-10

Universal counters

Operating principle



02/12/2010 6

Displayed result:

$$N_x = \frac{T_2}{T_1}$$ or $$N_x = f_1 T_2$$

Frequency measurement

The frequency f of a repetitive signal can be defined by the number of cycles of that signal per unit of time

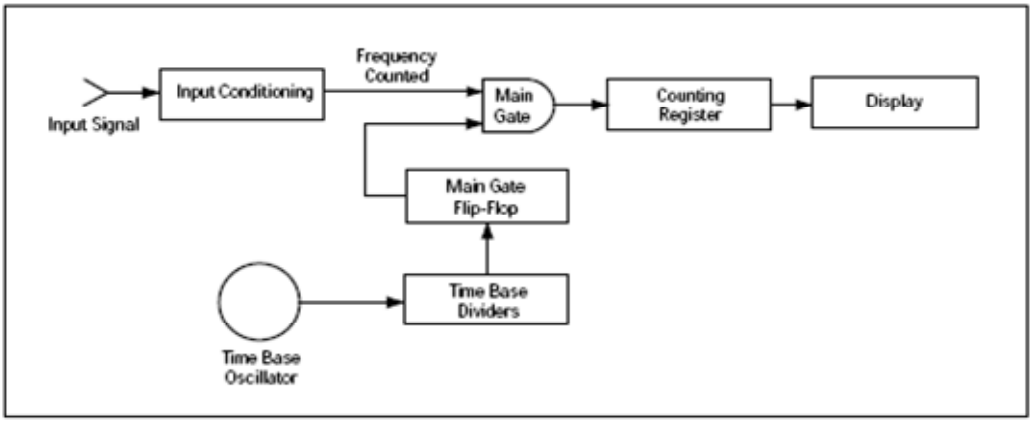
f=n/t,

where n is the number of cycles and t is the time interval in which they occur. As suggested by the above equation, the frequency can be measured by counting the number of cycles and dividing it by t. By taking t equal to one second, the number of counted cycles will represent the frequency (in Hz) of the signal.

The input signal is initially conditioned to a form that is compatible with the internal circuitry of the counter. The conditioned signal is a pulse train where each pulse corresponds to a cycle of the input signal. With the main gate open, pulses are allowed to pass through and get totalized by the counting register.

Universal counters

Basic block diagram of a universal counter in the frequency measurement mode



The time base oscillator together with the decade dividers and the main gate flip flop control the opening time of the main gate.

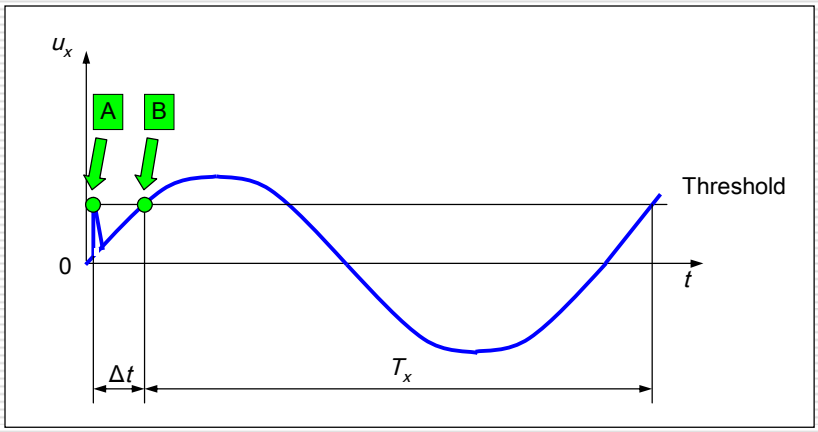
02/12/2010 10

10. *Universal counters. Trigger error for period measurements.*

https://intranet.etc.upt.ro/~E_INSTR/PowerPoint%20presentations%202010%202011/4%20Universal%20counters%202010%202011.ppt, slides #24-26

Errors of universal counters

Period measurement – trigger error



02/12/2010 24

Errors of universal counters

Trigger error

- for single period measurement

$$\delta_b = \frac{1}{\pi \cdot S/Z}$$

S/Z = signal to noise ratio

- for multiple period averaging

$$\delta_b = \frac{1}{N \cdot \pi \cdot S/Z}$$

02/12/2010 25

Errors of universal counters

Measurement uncertainty

- frequency meaurement

$$\delta_{fx\lim} = \delta_c + \delta_{osc}$$

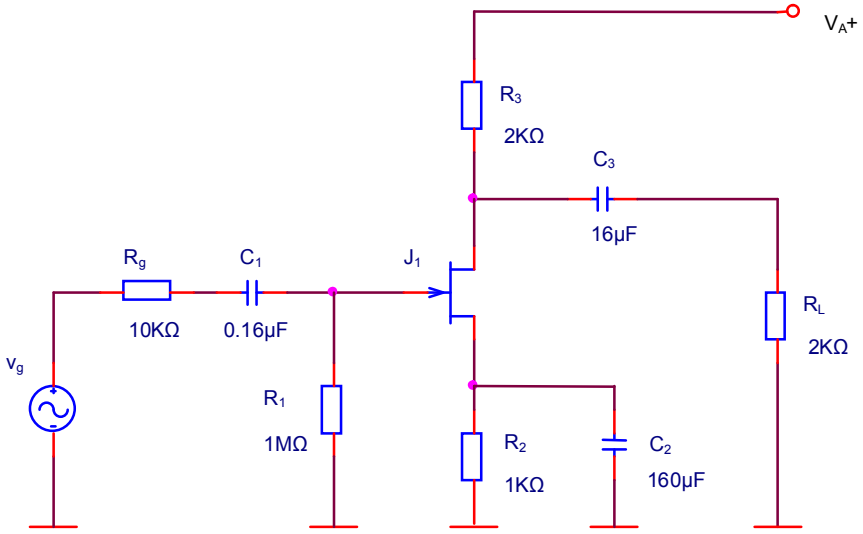
- period measurement

$$\delta_{Tx\lim} = \delta_c + \delta_{osc} + \delta_b$$

Fifth thematic area (apps)

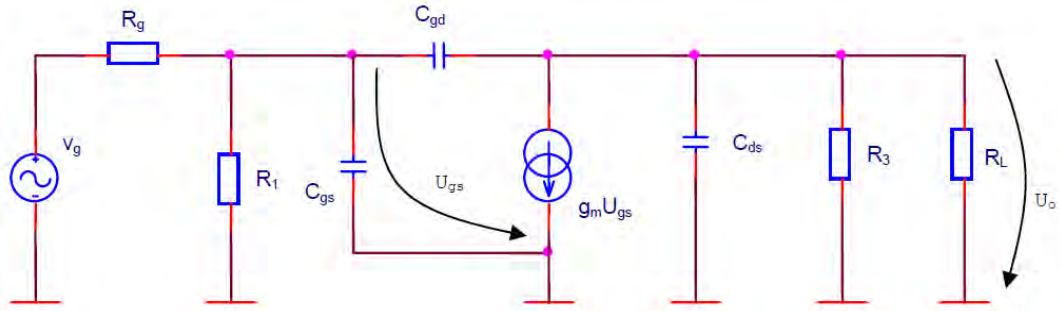
Electronic Circuits

1. **For the circuit below, having the J-FET with parameters: g_m = 5mA/V, r_{ds} = ∞, C_{gd} = 5pF, C_{gs} = 10pF, C_{ds} = 10pF.**
   Find out the high cutt off frequency by:
   a) Using Miller Theorem;
   b) Using OCTC (Open Circuit Time Constant) method.

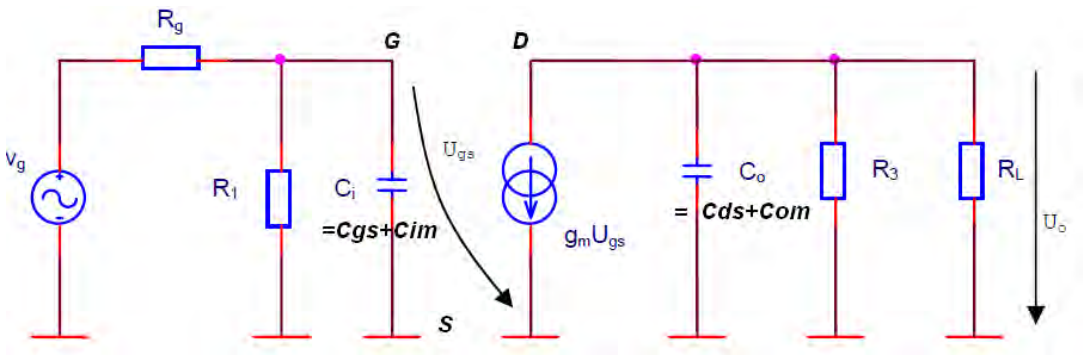


Solution:

a) First must draw equivalent schematic for small signal, mean frequencies:



By using Miller theorem, Cgd cand be splitted in 2 capacitors to ground Cim and Com, which will add to existing Cgs respective Cds, resulting in Ci and Co as below:



Gain *K* between G and D is needed to estimate Cim and Com capacitances:

$$K = \frac{U_o}{U_i} \text{ şi } U_o = -g_m U_{gs}(R_3 \| R_L),\ U_i = U_{gs} \Rightarrow \text{K} = A_{U0} = -g_{ms} R_3 \| R_L = -5$$

Then according to Miller:

$$C_{iM} = C_{gd}(1\text{-}K) = 30 \text{ pF},\ C_{oM} = C_{gd}\left(1 - \frac{1}{K}\right) = 6 \text{ pF}$$

$$C_i = C_{gs} \| C_{iM} = C_{gs} + C_{iM} = 40 \text{ pF},\ C_o = C_{ds} \| C_{oM} = C_{ds} + C_{oM} = 16 \text{ pF}$$

Cutt of (pole) frequencies introdeced by these capacitors are:

$$f_{P1} = \frac{1}{2 \cdot \pi \cdot C_i \cdot R_{P1}},\ R_{P1} = R_g \| R_1 \cong R_g \cong 10K\Omega \Rightarrow f_{P1} = 400KHz$$

$$f_{P2} = \frac{1}{2 \cdot \pi \cdot C_o \cdot R_{P2}},\ R_{P2} = R_3 \| R_L = 1K\Omega \Rightarrow f_{P2} = 10MHz\ .$$

Transfer function by neglecting zero frequency introduced by Cgs will be:

$$A_U(j\omega) = -5 \cdot \frac{1}{(1 + j\frac{f}{0.4 \cdot 10^6}) \cdot (1 + j\frac{f}{10 \cdot 10^6})}$$

High cutt of frequency will have aproximative value:

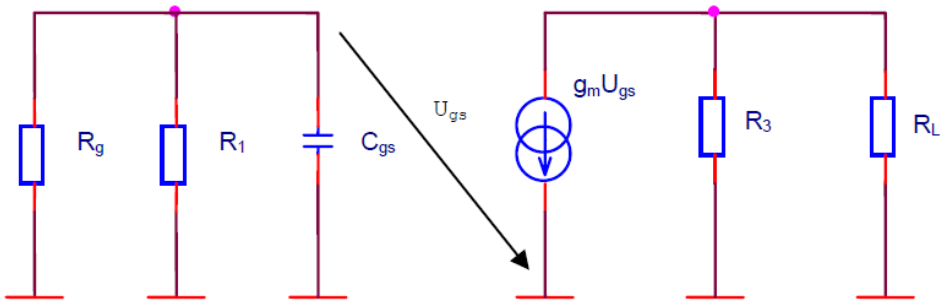
$$f_{P1} = 400\text{KHz}$$

Or can be computed exactly considering the 3db attenuation at cutt of frequency:

$$\left|A_U(j\omega)\right|_{f=f_{\hat{i}}} = \frac{1}{\sqrt{2}} A_{U0} \Rightarrow f_{\hat{i}} = 393{,}7\text{KHz}$$

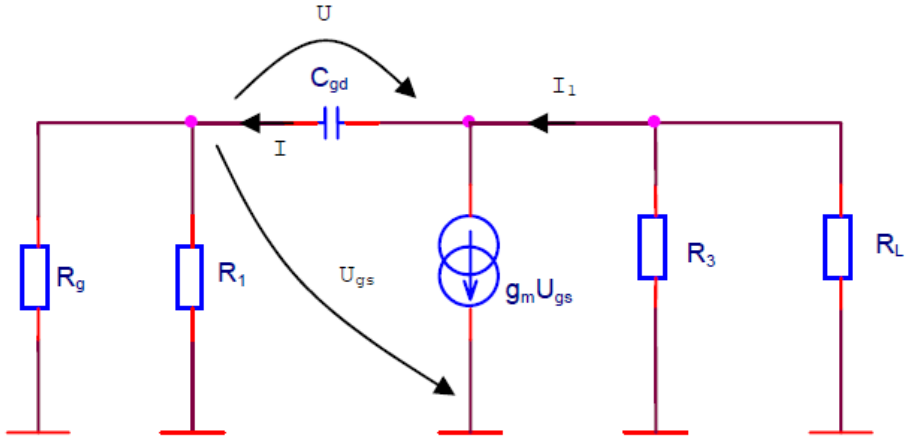
b) If OCTC is applied to first schematic (without to get benefit of Miller theoreme), involve to evaluate 3 time constants, one for each capacitor as folows:

- **Cgs effect**, all the others C = open circuit:



$$f_{P1} = \frac{1}{2 \cdot \pi \cdot C_{gs} \cdot R_{P1}}, R_{P1} = R_1 \| R_g \cong R_g \cong 10K \Rightarrow f_{P1} = 1{,}6MHz$$

- **Cgd effect**, all the others C = open circuit:



$$f_{P2} = \frac{1}{2 \cdot \pi \cdot C_{gd} \cdot R_{P2}}$$

Equivalent resistance between Cgd nodes can be found if Cgd is replaced with a voltage source U:

$$R_{P2} = \left| \frac{U}{I} \right|$$

Using Kirchhoff laws :

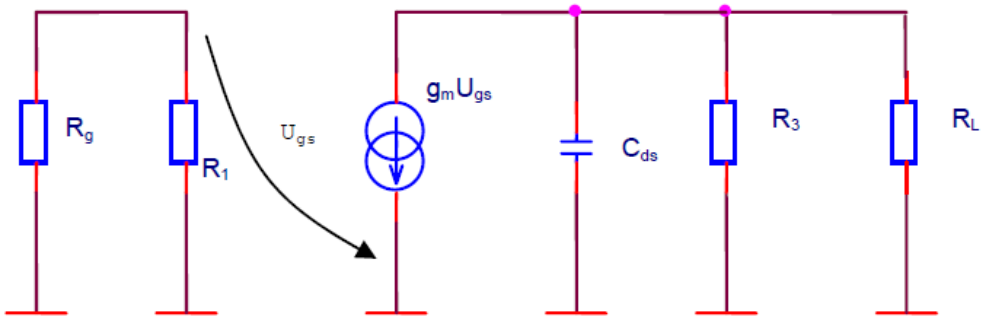
$$-i \cdot R_g \| R_1 + u_{gs} = 0 \Rightarrow u_{gs} = i \cdot R_g \| R_1$$

$$I_1 = g_m \cdot u_{gs} + I = I(1 + g_m \cdot R_g \| R_1)$$

$$U - I \cdot R_g \| R_1 - I_1 \cdot R_3 \| R_L = 0 \Rightarrow U = I \cdot R_g \| R_1 + I \cdot (1 + g_m \cdot R_g \| R_1) \cdot R_3 \| R_L$$

$$R_{P2} = \frac{U}{I} = R_g \| R_1 + (1 + g_m \cdot R_g \| R_1) \cdot R_3 \| R_L = 61\text{K}\Omega. \Rightarrow f_{P2} = 524{,}6KHz$$

- **Cds effect**, all the others C = open circuit:



$$f_{P3} = \frac{1}{2 \cdot \pi \cdot C_{ds} \cdot R_{P3}},\ R_{P3} = R_3 \| R_L = 1K \Rightarrow f_{P3} = 16MHz$$

According to SCTC:

$$\frac{1}{f_i} = \frac{1}{f_{i1}} + \frac{1}{f_{i2}} + \frac{1}{f_{i3}} \Rightarrow f_i \cong 385{,}2KHz.$$

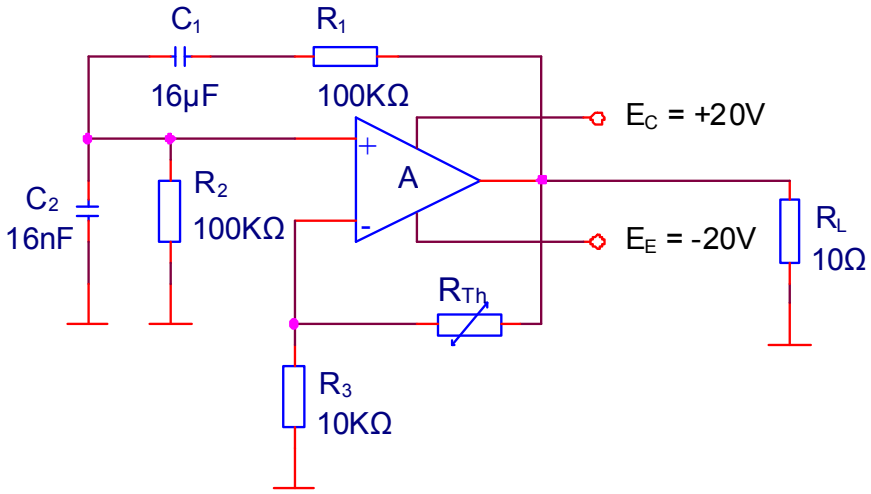
close to the value obtained at a)

2. **The schematic below is a Wien oscillator using a class B final stage amplifier having: $A_u \to \infty$, $R_i \to \infty$, $R_o \to 0$. Find out:**

a) f_0 oscillating frequency,

b) V_0, when using the thermistor R_{Th};

c) P_0 (delivered to R_L)



Solution:

a) $f_o = \frac{1}{2 \cdot \pi \cdot \sqrt{R_1 R_2 C_1 C_2}} \cong 100Hz$

b) $A = 1 + R_{Th}/R_3$, and at f_0: $|\beta| = 1/3$.

From $|A||\beta| = 1 \Rightarrow R_{Th} = 20K\Omega$ obtained for $U_{Th} = 10V$.
Feedback topology is series-shunt, actually a voltage divider including R_{Th}, so:

$$u_{Rth} = u_o \cdot \frac{R_{Th}}{R_{Th} + R_3} = \frac{2}{3} \cdot u_o \Rightarrow u_o = 1{,}5 \cdot u_{Rth} = 15V_{ef}$$

$$u_{om} = \sqrt{2} \cdot 15V_{vv}$$

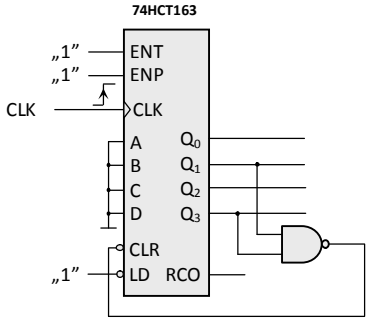
c)

$$P_o = \frac{u_{om}^{\ 2}}{2 \cdot R_L} = 22{,}5W$$

Digital Integrated Circuits

3. Use a 74x163 binary synchronous counter (with synchronous reset) to design a modulus 11 counter (the counting sequence is: 0, 1, 2... 10, 0, 1, 2, ...). Explain what happens if the reset is asynchronous.

Solution: A 2-input NAND gate is used to detect the 10 state ($Q_3Q_2Q_1Q_0$ = 1010) and by clearing the counter the next state will be 0000. A different modulus is obtained if the reset is asynchronous. The Preset inputs (A, B, C, D) and the nLD input are not used.



4. Using 27C256 EPROM memories (32k x 8 bit) and glue logic, design a 64k x 8 bit memory.

Solution: a). The number of EPROM circuits is:

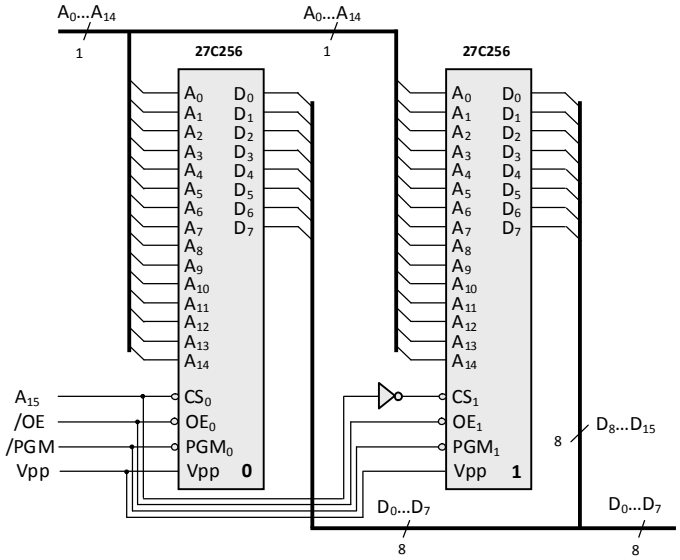
$$N = \frac{64k\,x\,8}{32k\,x\,8} = 2\,.$$

b). The initial memory has 15 address lines ($A_0 \ldots A_{14}$). The final memory has 16 address lines.

A_{15}	$A_{14} - A_0$	Memory #	Enable	
			$\overline{CS_0}$	$\overline{CS_1}$
0	X….. X	0	0	1
1	X….. X	1	1	0

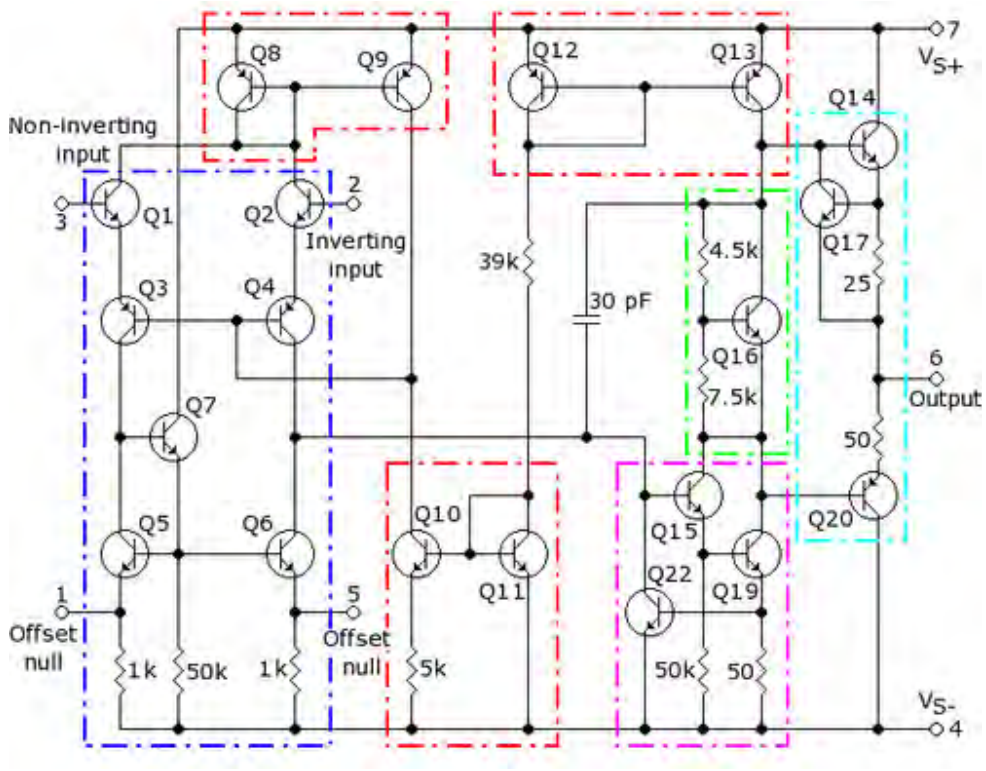
A15 is used to select one of the two memories. One inverter is associated with this task. The two memories have a common address bus $A_0 \ldots A_{14}$ and a common data bus $D_0, \ldots, D_7$. oOE, nPGM and Vpp are also connected together.

The final schematic is:



Analog Integrated Circuits

5. Name the building blocks inside the op. amp. shown in the figure.



Solution:

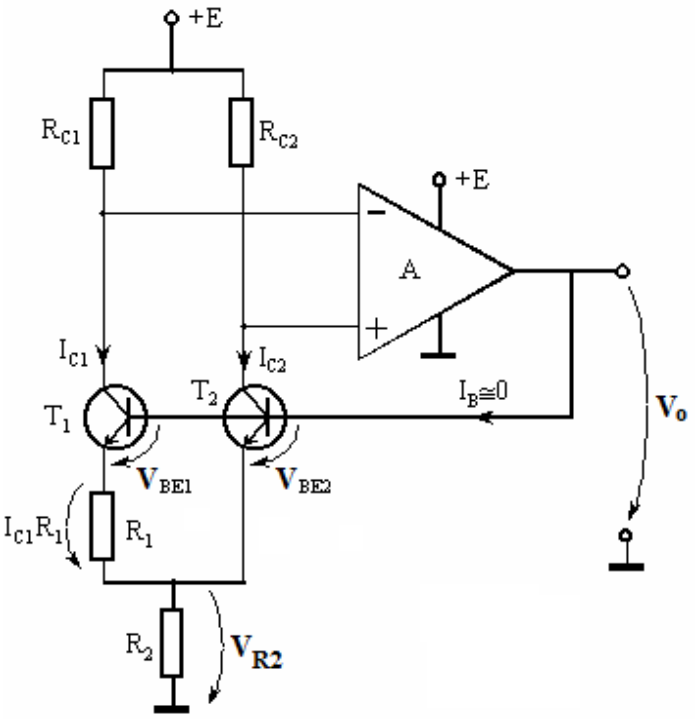
At the left-hand side of the figure, the first block is a differential input stage with emitter followers (*Ql* and *Q2*) driving common-base stages (*Q3* and *Q4*). The transistors *Q5* and *Q6* form an active load for *Q3* and *Q4*. Transistors *Q7*, *Q5*, *Q6* and their emitter resistances form a simple current mirror with degeneration. The two pairs of transistors shown at the top of the schematic are simple current mirrors (*Q8* and *Q9*, *Q12* and *Q13*). At the bottom is a Widlar current source (built by *Q10*, *Q11*, and the 5 kΩ resistor). Transistors *Q15*, *Q19* and *Q22* operate as a class A gain stage. The stage consists of two NPN transistors in a Darlington configuration (*Q15* and *Q19*). Transistor *Q16* and its base resistors is the V_{be} multiplier voltage source. Transistors *Q14*, *Q20* form the class AB push-pull emitter follower output stage.

6. A band-gap-referenced bias circuit is shown in the figure. T_1 and T_2 are identical. The ratio of R_{C1} to R_{C2} is 2: $R_{C1}/R_{C2} = 2$ and $R_1 = 2.6$ KΩ.

a. Calculate the output voltage, V_o and prove that it is possible to have a voltage reference.

b. b). Calculate the value of the currents I_{C1} and I_{C2}.

You have: ln2 = 0.693; ln5 = 1.6; ln10=2.3; V_T=26mV at 300 K.



Solution:

We consider an ideal op. amp. $\Rightarrow \quad V_{R_{C1}} = V_{R_{C2}} \Leftrightarrow I_{C1}R_{C1} = I_{C2}R_{C2} \Rightarrow \dfrac{I_{C2}}{I_{C1}} = \dfrac{R_{C1}}{R_{C2}} = 2 \quad (1)$

KVL in the loop of R_1 and two V_{BE}:

$$V_{BE1} + I_{C1}R_1 = V_{BE2} \Leftrightarrow I_{C1}R_1 = V_{BE2} - V_{BE1} = V_T \ln\frac{I_{C2}}{I_{S2}} - V_T \ln\frac{I_{C1}}{I_{S1}}$$

But T_1 and T_2 are identical $\Rightarrow I_{S1} = I_{S2} \Rightarrow I_{C1}R_1 = V_T \ln\dfrac{I_{C2}}{I_{C1}} = V_T \ln 2 \Rightarrow I_{C_1} = \dfrac{V_T \ln 2}{R_1}$ (2)

$$V_o = V_{BE2} + V_{R_1} = V_{BE2} + (I_{C1} + I_{C2})R_2 \quad (3)$$

$$\overset{(3),(1)}{\Rightarrow} V_o = V_{BE2} + (I_{C1} + 2I_{C1}) \cdot R_2 \overset{(2)}{=} V_{BE2} + 3 \cdot R_2 \cdot \frac{V_T \ln 2}{R_1} = V_{BE2} + \left(3 \cdot \frac{R_2}{R_1} \cdot \ln 2 \right) \cdot V_T$$

V_o will be compensated if $3 \cdot \frac{R_2}{R_1} \cdot \ln 2 = N = 23 \Rightarrow R_2 = \frac{23 \cdot R_1}{3 \cdot \ln 2} \Rightarrow R_2 = \frac{23 \cdot 2.6 \cdot 10^3}{3 \cdot 0.693} = 28.7k\Omega$

So, if $R_2 = 28.7k\Omega$ we have a band-gap referenced circuit and the output voltage is:

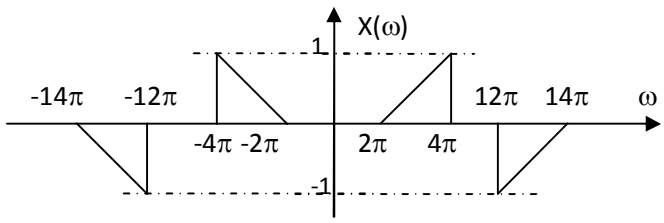
$$V_o = V_{BE} + N \cdot V_T \cong 0.6V + 23 \cdot 26mV = 1.198V$$

b) $I_{C1} = \frac{V_T \ln 2}{R_1} = \frac{26 \cdot 10^{-3} \cdot 0.693}{2.6 \cdot 10^3} \cong 0.7\mu A$

$$I_{C2} = 2 \cdot I_{C1} = 14\mu A$$

Signal Processing

7. Consider the signal $x(t)$ with the spectrum below



What is the minimum sampling frequency $f_{s\min}$ according to the sampling theorem?

Solution:

$$f_{s\min} = 2f_M = 2\square 7Hz = 14Hz$$

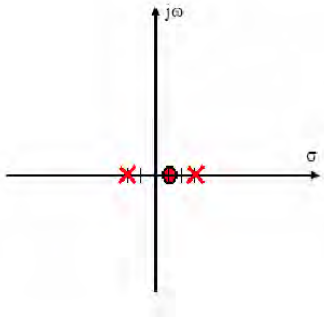
$$f_M = \frac{14\pi rad/s}{2\pi rad} = 7Hz$$

8. **Consider the system with the transfer function** $H(s)=\dfrac{s-1}{(s+2)(s-3)}$.

Sketch its pole/zero plot.

Solution:

$$X(s)=\frac{s-1}{(s+2)(s-3)}$$



x- pole

o – zero

Electronic Instrumentation

9. **The 50 ns rise time of a square wave (t_{ri}) read on the screen of an oscilloscope (t_{ro}) is 60 ns. Determine the oscilloscope's bandwidth! Round it off to the nearest standard value (10, 20, 35, 40, 50, 60, 75, 100, 150, 250, 300, 500 MHz)!**

Solution:

Using the equation $t_{ro}^2=t_{ri}^2+t_r^2$, the rise time of the oscilloscope is found to be

$$\sqrt{3600-2500}=\sqrt{1100}\ \ =33.16ns$$

The bandwidth is

$$B=\frac{350}{t_r}=\frac{350}{33.16}=10.55MHz$$

The nearest standard value is 10 MHz.

10. An universal counter displays 100.100 kHz when measuring the frequency of an input signal. Determine the quantization error in Hz, % and ppm! (remember, "." is the decimal point)

Solution:

The quantization error is 1 Hz (one least significant digit)

or, in percent

$$1 \text{ Hz} / 100100 \text{ Hz} \times 100 = 0.001\%$$

or, in ppm

$$1 \text{ Hz} / 100100 \text{ Hz} \times 1{,}000{,}000 = 10 \text{ ppm.}$$

Radio Communications

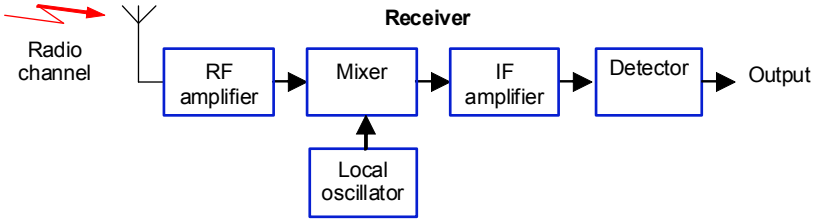
1. Draw and explain the main blocks of a radio receiver.

Course nb.1 slide 12.

Site address: https://intranet.etc.upt.ro/~RADIOCOM/

Answer:

The receiver block incorporate many amplifier and processing stages, and one of the most important is the oscillator stage.



The receiver oscillator is called the local oscillator as it produces a local carrier within the receiver which allows the incoming carrier from the transmitter to be down converted for easier processing within the receiver. The mixer and the IF amplifier are used to extract the intermediate frequency. The user information is obtained after detection.

2. What wavelength corresponds to a frequency of 600 MHz?

Course nb.2 slide 45.

Site address: https://intranet.etc.upt.ro/~RADIOCOM/

Answer:

$\lambda = c/f = (3x10^8 m/s)/(6x10^8 Hz) = 0.5$ m

3. What are the radiation regions of an antenna?

Course nb.3 slide 36-39.

Site address: https://intranet.etc.upt.ro/~RADIOCOM/

Answer:

The antenna radiation field is divided into:

- reactive near-field (objects within this region will result in coupling with the antenna and distortion of the ultimate far-field antenna pattern),

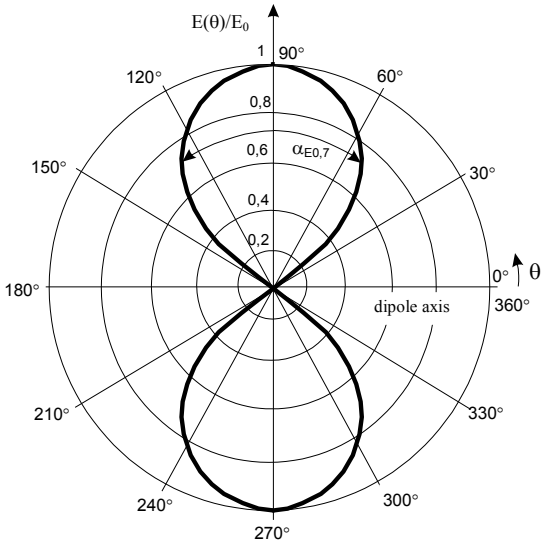
- radiating near-field (transition region),

- far-field (the gain of the antenna is a function only of angle).

4. Describe the directivity of a half-wave dipole antenna.

Course nb.4 slide 35-36.

Site address: https://intranet.etc.upt.ro/~RADIOCOM/



Answer:

A half-wave dipole has an antenna gain of 1.64 or $G = 2.15$ dBi.

It has an Omni directional pattern in the H-plane.

In E-plane the directivity is bidirectional.

5. What represents the array factor?

Course nb.5 slide 15-16.

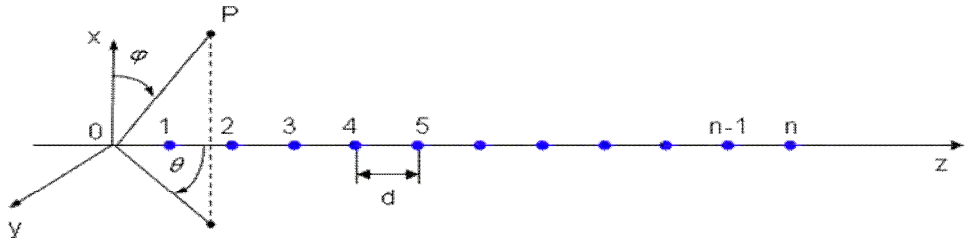
Site address: https://intranet.etc.upt.ro/~RADIOCOM/

Answer:

An array of antennas working simultaneously can focus the reception or transmission of energy in a particular direction, which increases the useful range of a system.

The array influence is contained inside of an array factor AF:

Array pattern = Element pattern x Array factor

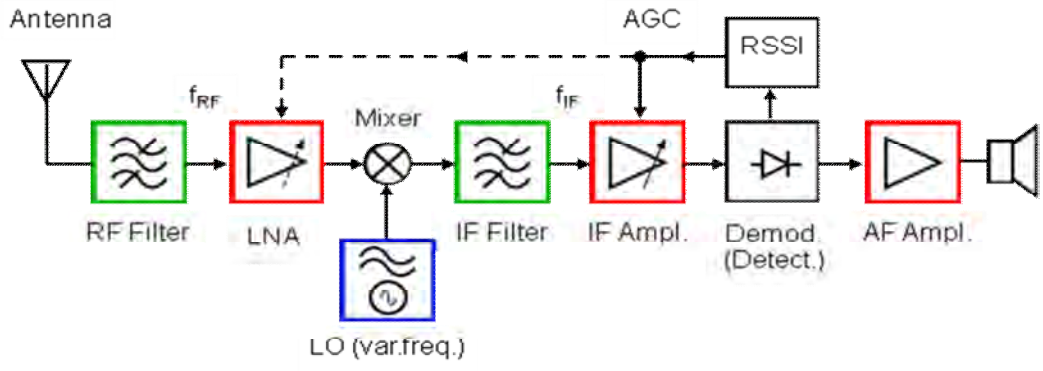


6. Draw and explain the main blocks of a superheterodyne receiver.

Course nb.6 slide 9-11.

Site address: https://intranet.etc.upt.ro/~RADIOCOM/

Answer:



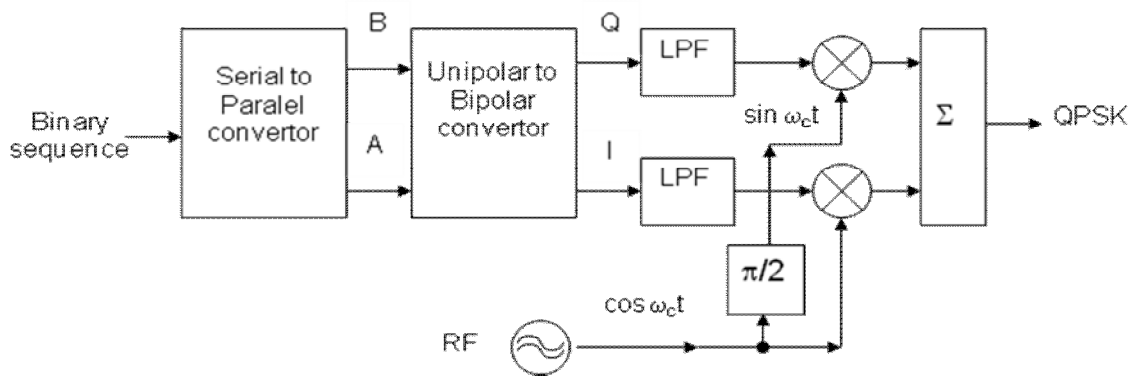
The RF front end consists in a band-pass filter and low-noise amplifier for radio bandwidth selection. The local oscillator and the mixer followed by an IF filter are used for heterodyne process performing channel selection. IF blocks amplify the signal to ensure the right level at the demodulator input. An automatic gain control loop is used to maintain a constant level in case of fading.

7. Draw and explain the QPSK modulator.

Course nb.7 slide 33-34.

Site address: https://intranet.etc.upt.ro/~RADIOCOM/

Answer:



The baseband coding of information consists first in parallel conversion. The two streams resulted are converted in bipolar signals with a symbol duration being twice the bit duration. Each of them is low-pass filtered and used to modulate in phase a RF carrier. The two carriers have a 90^o phase shift to be orthogonal. The result is a constant amplitude signal with 4 possible states of its phasor (4 state constellation).

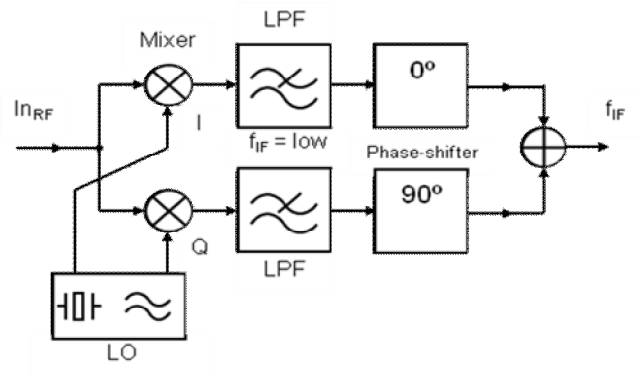
8. Explain the image reject mixer with Hartley architecture.

Course nb.8 slide 17-23.

Site address: https://intranet.etc.upt.ro/~RADIOCOM/

Answer:

The principle of image-rejection is to process the desired channel and its image in such a way that the image can be eliminated eventually by *signal cancellation*.



The RF signal in the downconversion is split into two components by using two matched mixers and quadrature LO signals.

The resulting IF signals, namely in phase (I) and quadrature phase (Q), are then lowpass-filtered and after one is phase-shifted by 90°, the IF signals are combined.

In this process, depending on the IF path that is subjected to the 90° phase-shifter, either the image band or the receive band is cancelled after the summation of I and Q outputs.

9. Define the receiver's selectivity.

Course nb.9 slide 19.

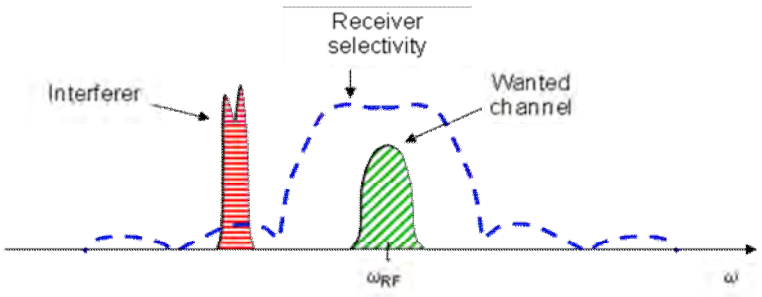
Site address: https://intranet.etc.upt.ro/~RADIOCOM/

Answer:

A receiver's selectivity performance is a measure of the ability to separate the desired band about the carrier, from unwanted interfering signals received at other frequencies.

This situation is most often characterized by a weak received desired signal in the presence of a strong adjacent or alternate band user.

Receiver selectivity may be defined also as the ability to reject unwanted signals on adjacent channel frequencies.



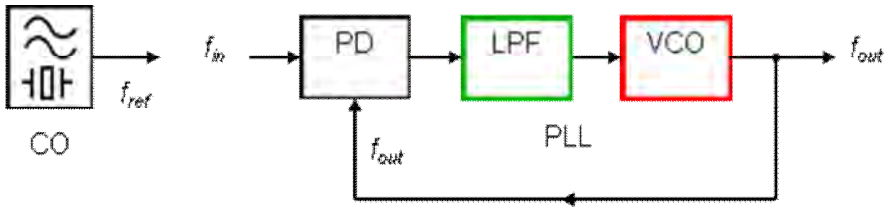
10. Which are the major components of the PLL (Phase-locked loop) frequency synthesizer?

Course nb.10 slide 27-29.

Site address: https://intranet.etc.upt.ro/~RADIOCOM/

Answer:

A PLL is a circuit which causes a particular system to track with another one. More precisely, a PLL is a circuit synchronizing an output signal (generated by an oscillator) with a reference or input signal in frequency as well as in phase.



The major components are the Phase Detector (PD), the LPF = Loop Filter (Low-pass filter LPF), and the Voltage-controlled oscillator (VCO).

Power Electronics

1. *Define the total harmonic distortion coefficient (THD) and the power factor (PF). Power factor formula for sinusoidal input voltage and nonlinear load.*

Given a periodic signal *x(t)*, the *total harmonic distortion coefficient* (THD) is defined as:

$$THD = \frac{rms\ value\ without\ fundamental}{rms\ fundamental} = \frac{\sqrt{X_0^2 + \frac{1}{2}\sum_{n=2}^{\infty} X_n^2}}{\frac{X_1}{\sqrt{2}}}$$

where X_0 is the dc component and X_n are the amplitudes of harmonics.

For efficient transmission of energy from a source to a load, it is desired to *maximize average power*, while *minimizing rms current and voltage* (and hence minimizing losses). The *power factor* (*PF*) is a *figure of merit* that measures how energy is efficiently transmitted. It is defined as the ratio between average power and apparent power:

$$PF = \frac{P}{S}\frac{P}{V_{rms}\cdot I_{rms}} = \frac{\int_{t_0}^{t_0+T} v(t)\cdot i(t)dt}{\sqrt{\frac{1}{T}\int_{t_0}^{t_0+T} v(t)^2 dt}\cdot\sqrt{\frac{1}{T}\int_{t_0}^{t_0+T} i(t)^2 dt}} \qquad (1)$$

With a sinusoidal voltage, current harmonics do not lead to average power. However, current harmonics do increase the rms current, and hence they decrease the power factor.

As with a sinusoidal voltage $P = \frac{1}{2}V_1 I_1 \cos(\varphi_1 - \theta_1)$; $V_{rms} = \frac{V_1}{\sqrt{2}}$; $I_{rms} = \sqrt{I_0^2 + \frac{1}{2}\sum_{n=2}^{\infty} I_n^2}$

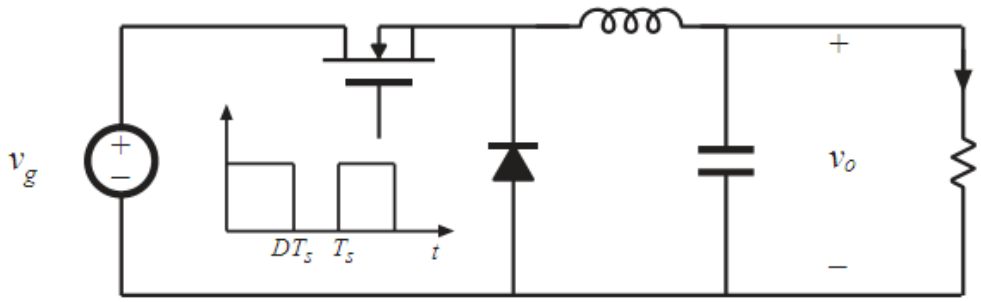
from (1) it results that: $PF = \frac{\frac{I_1}{\sqrt{2}}}{\sqrt{I_0^2 + \frac{1}{2}\sum_{n=2}^{\infty} I_n^2}}\cdot\cos(\varphi_1 - \theta_1) = K_{di}\cdot K_\theta$

where: $K_{di} = \frac{\frac{I_1}{\sqrt{2}}}{\sqrt{I_0^2 + \frac{1}{2}\sum_{n=2}^{\infty} I_n^2}}$ - current distortion factor

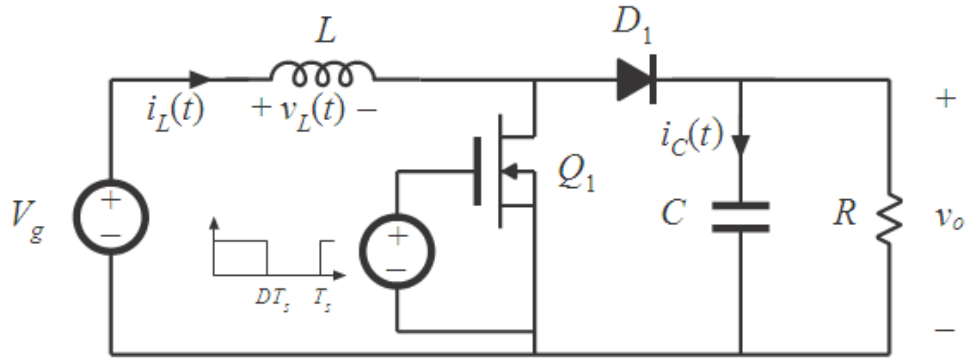
and $K_\theta = \cos(\varphi_1 - \theta_1)$ = displacement factor

$PF = Current\ distortion\ factor \cdot Displacement\ factor$

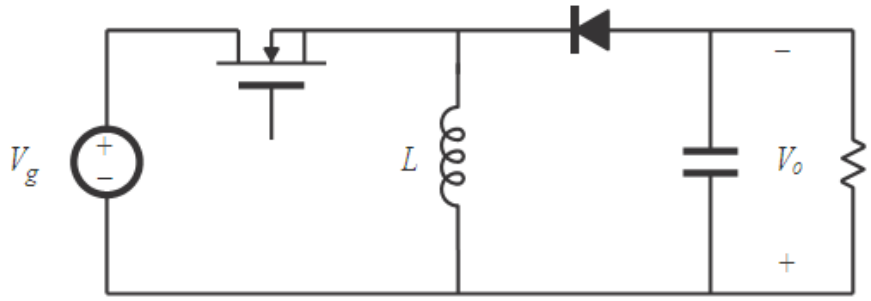
2. *The four basic dc-dc nonisolated converters: buck, boost, buck-boost, Ćuk: schematics with practical semiconductors and their static conversion ratios values.*



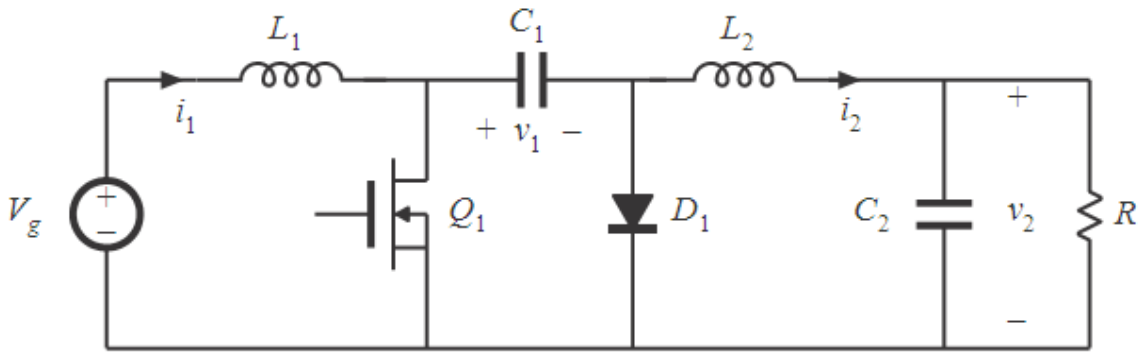
Buck converter. $M(D) = D$



Boost converter. $M(D) = \dfrac{1}{1-D}$

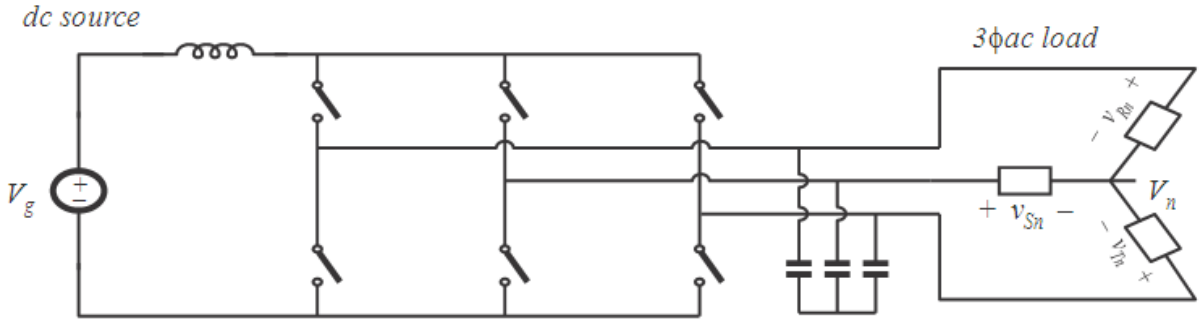


Buck-Boost converter. $M(D) = \dfrac{D}{1-D}$

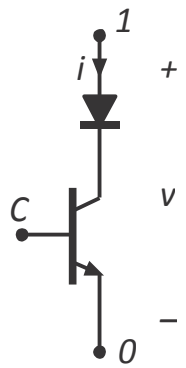


Ćuk converter. $M(D) = \frac{D}{1-D}$

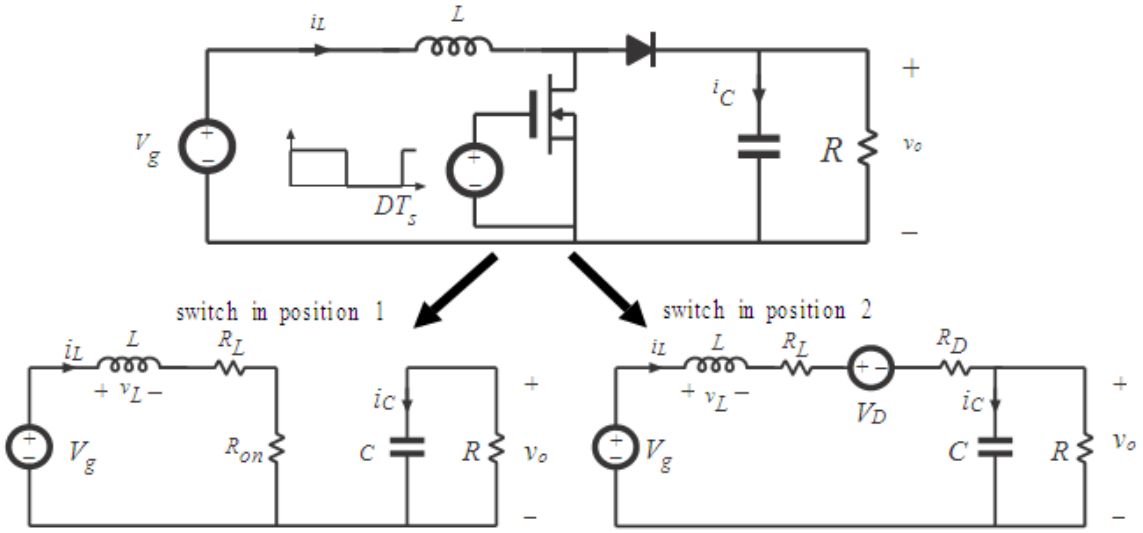
3. The three phase current source inverter – schematics, characteristic nature, switch implementation.



Exhibits a *boost-type* conversion characteristic. The switches are current unidirectional (voltage bidirectional) two quadrant switches, such as:



4. ***Nonideal converters analysis. Literally calculate the static conversion ratio*** M ***and efficiency*** η ***of a boost converter taking into account inductor series resistance*** R_L ***and semiconductor conduction losses: transistor on resistance*** R_{on} ***and diode forward voltage drop*** V_D***. Use small ripple assumption together with volt-second balance and charge balance equations. At what duty cycles efficiency becomes poor when only transistor conduction losses are taken into account?***



Small-ripple assumption: inductor current i_L and capacitor voltage v_o have negligible ripple and therefore they may be assumed as constant, denoted by capitals, I_L, V_o.

Volt- second balance equation:

$$D(V_g - I_L R_L - I_L R_{on}) + (1-D)(V_g - I_L R_L - V_D - I_L R_D - V_o) = 0 \qquad (1)$$

Charge balance equation:

$$D\left(-\frac{V_o}{R}\right) + (1-D)\left(I_L - \frac{V_o}{R}\right) = 0 \qquad (2)$$

Equations (1) and (2) together are a linear system with I_L and V_o as unknowns.

Solve for *M*. Final result is:

$$M = \frac{1}{1-D} \cdot \frac{1-\frac{V_D}{V_g}}{1+\frac{1}{(1-D)^2}\cdot\frac{R_L}{R}+\frac{D}{(1-D)^2}\cdot\frac{R_{on}}{R}+\frac{1}{1-D}\cdot\frac{R_D}{R}} \tag{3}$$

Now efficiency can be estimated as output to input average powers ratio:

$$\eta = \frac{P_o}{P_g} = \frac{\frac{V_0^2}{R}}{V_g I_L} \tag{4}$$

On the other side, from (2) $I_L = \frac{V_0}{R(1-D)}$ and substituting in (4) one obtains:

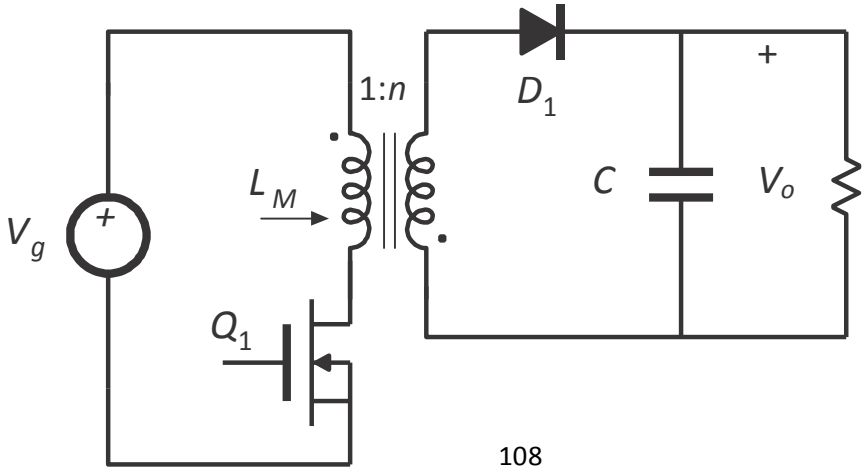
$$\eta = (1-D)\frac{V_o}{V_g} = (1-D)M \overset{(1)}{=} \frac{1-\frac{V_D}{V_g}}{1+\frac{1}{(1-D)^2}\cdot\frac{R_L}{R}+\frac{D}{(1-D)^2}\cdot\frac{R_{on}}{R}+\frac{1}{1-D}\cdot\frac{R_D}{R}} \tag{5}$$

When only transistor conduction losses are taken into account efficiency formula form (5) becomes ($R_L = R_D = 0$, $V_D = 0$):

$$\eta = \frac{1}{1+\frac{D}{(1-D)^2}\cdot\frac{R_{on}}{R}} = \eta(D) \tag{6}$$

As $\eta(0) = 1$ and $\lim\limits_{\substack{D\to 1\\ D<1}} \eta(D) = 0$ it is clear that efficiency becomes poor at high duty cycles.

5. The flyback converter: schematics, static conversion ratio, applications, advantages and limitations.



$$M(D) = n\frac{D}{1-D} = n\frac{D}{D'}$$

- ✓ Widely used in low power and/or high voltage applications
- ✓ Low parts count
- ✓ Multiple outputs are easily obtained, with minimum additional parts
- ✓ Often operated in discontinuous conduction mode
- ✓ Cross regulation is inferior to buck-derived isolated converters

6. *The classical single-transistor forward converter: schematics, main waveforms, maximum duty cycle.*

From magnetizing current volt-second balance

$$DV_g + (D_2)(-\frac{n_1}{n_2}V_g) + D_3 \cdot 0 = 0$$

Solve for D_2:

$$D_2 = \frac{n_2}{n_1}D$$

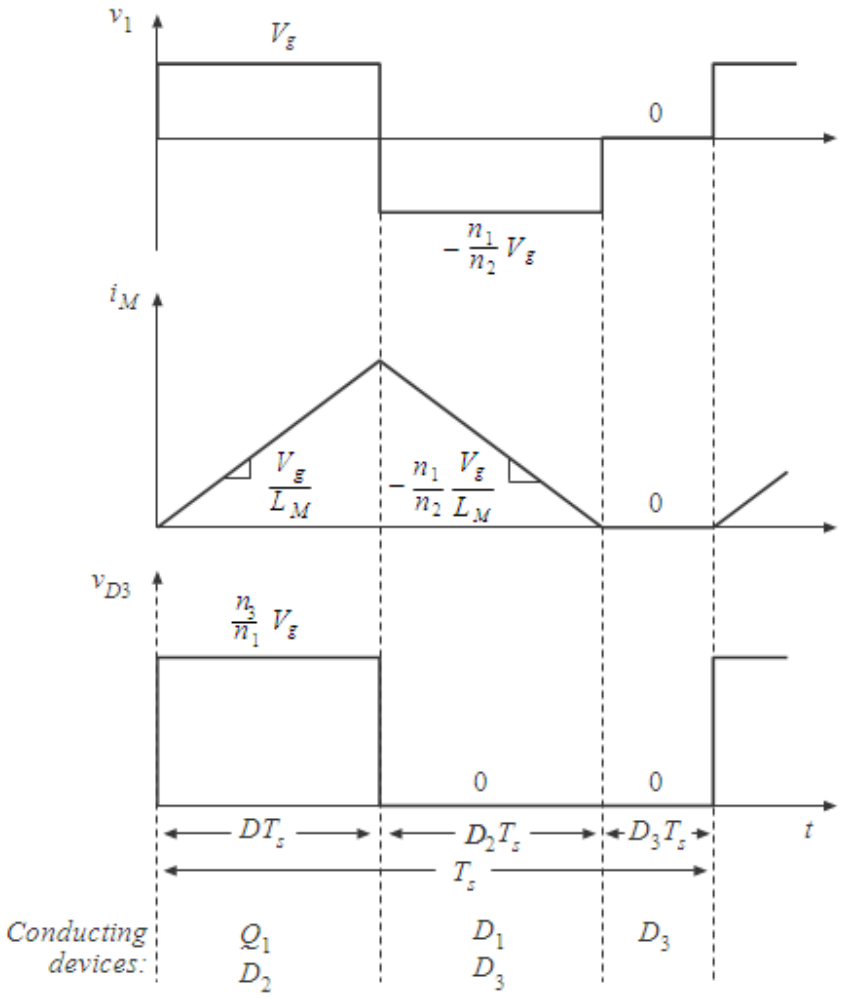
D_3 cannot be negative. But $D_3 = 1 - D_2 - D$. Hence, using the value for D_2 previously obtained, it follows that:

$$1 - \frac{n_2}{n_1}D - D \geq 0\,,$$

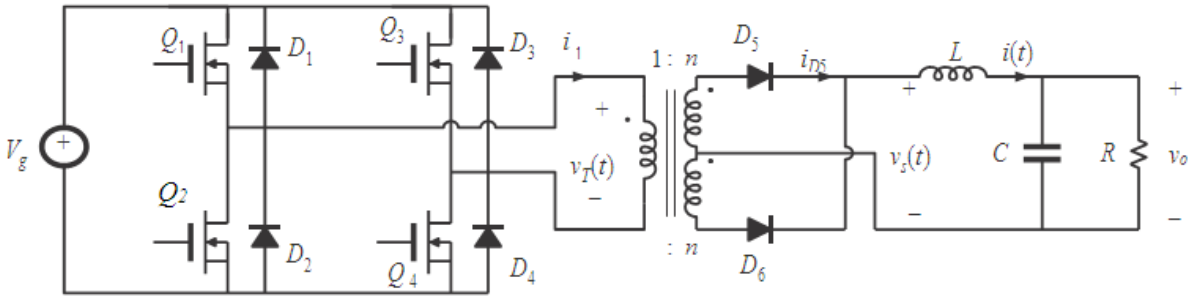
finally resulting in

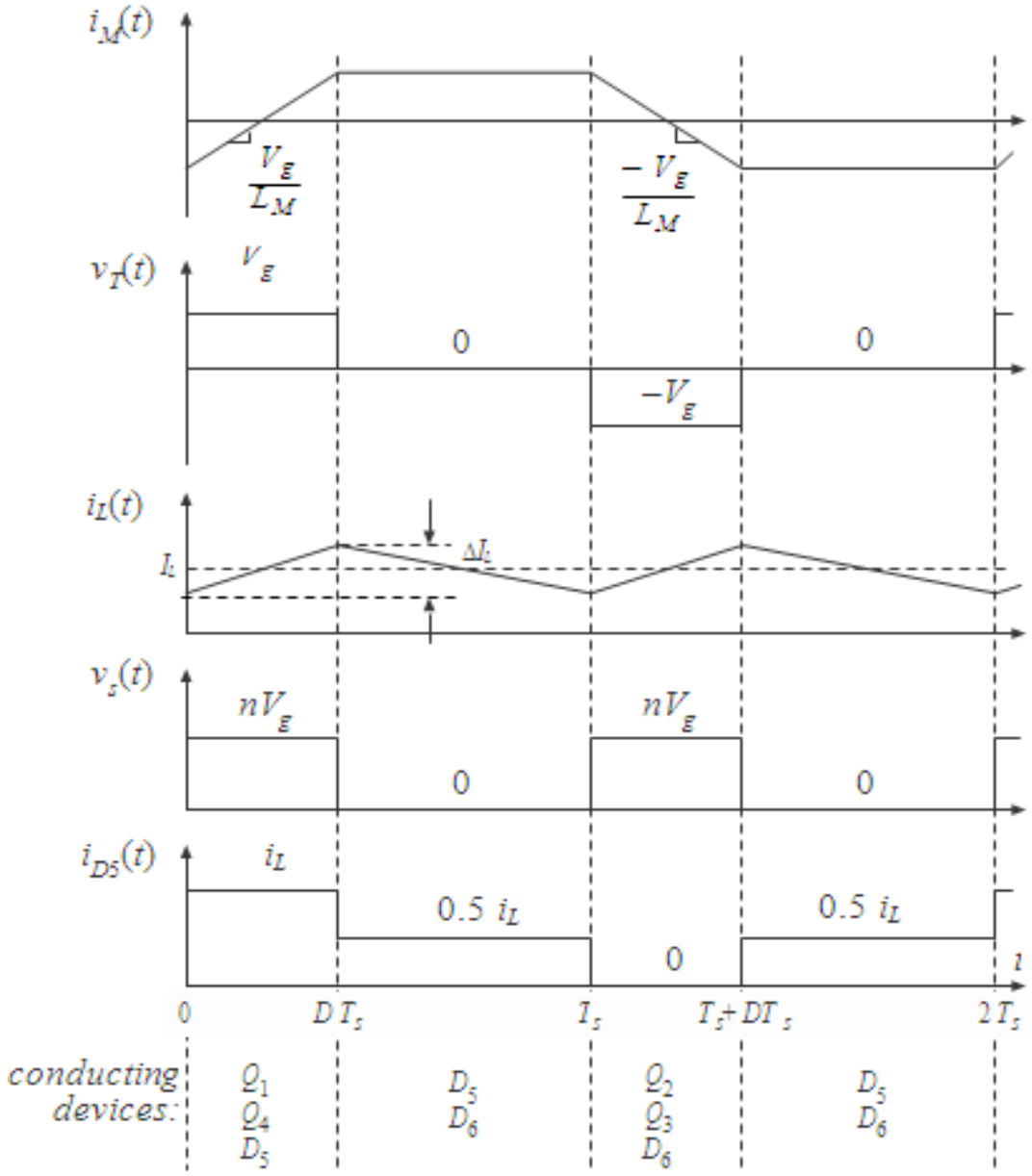
$$D \leq \frac{1}{1+\frac{n_2}{n_1}}$$

If the final result is provided without proof the anwer will also be accepted.



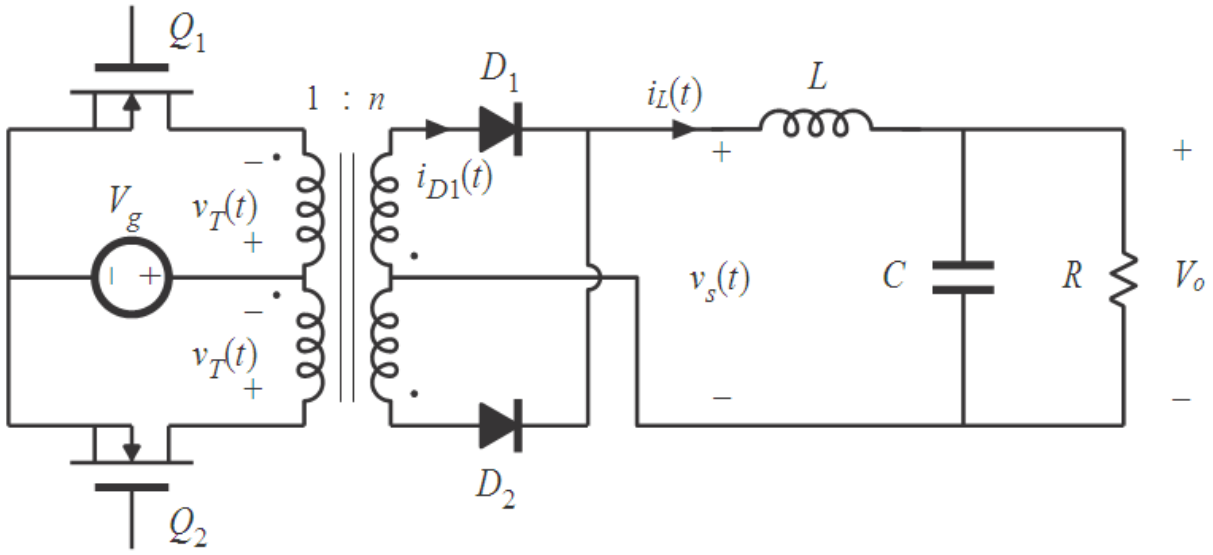
7. The full-bridge isolated buck converter: schematics, main waveforms, solutions for preventing core saturation.





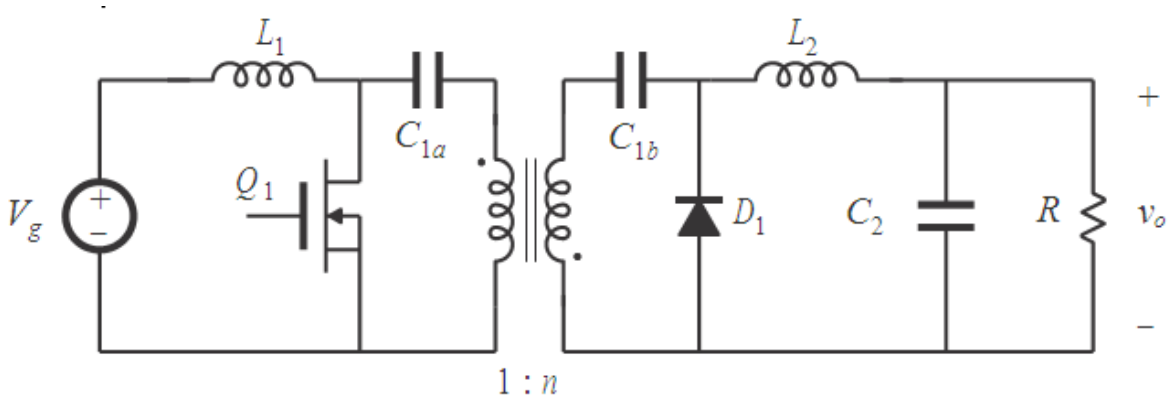
Saturation can be prevented by placing a *capacitor* in series with primary or by use of the so called *current programmed mode.*

8. *Push-pull isolated buck and isolated Ćuk converters: schematics, type of control, advantages and disadvantages regarding transformer magnetizing current.*



Push-pull isolated buck-derived converter

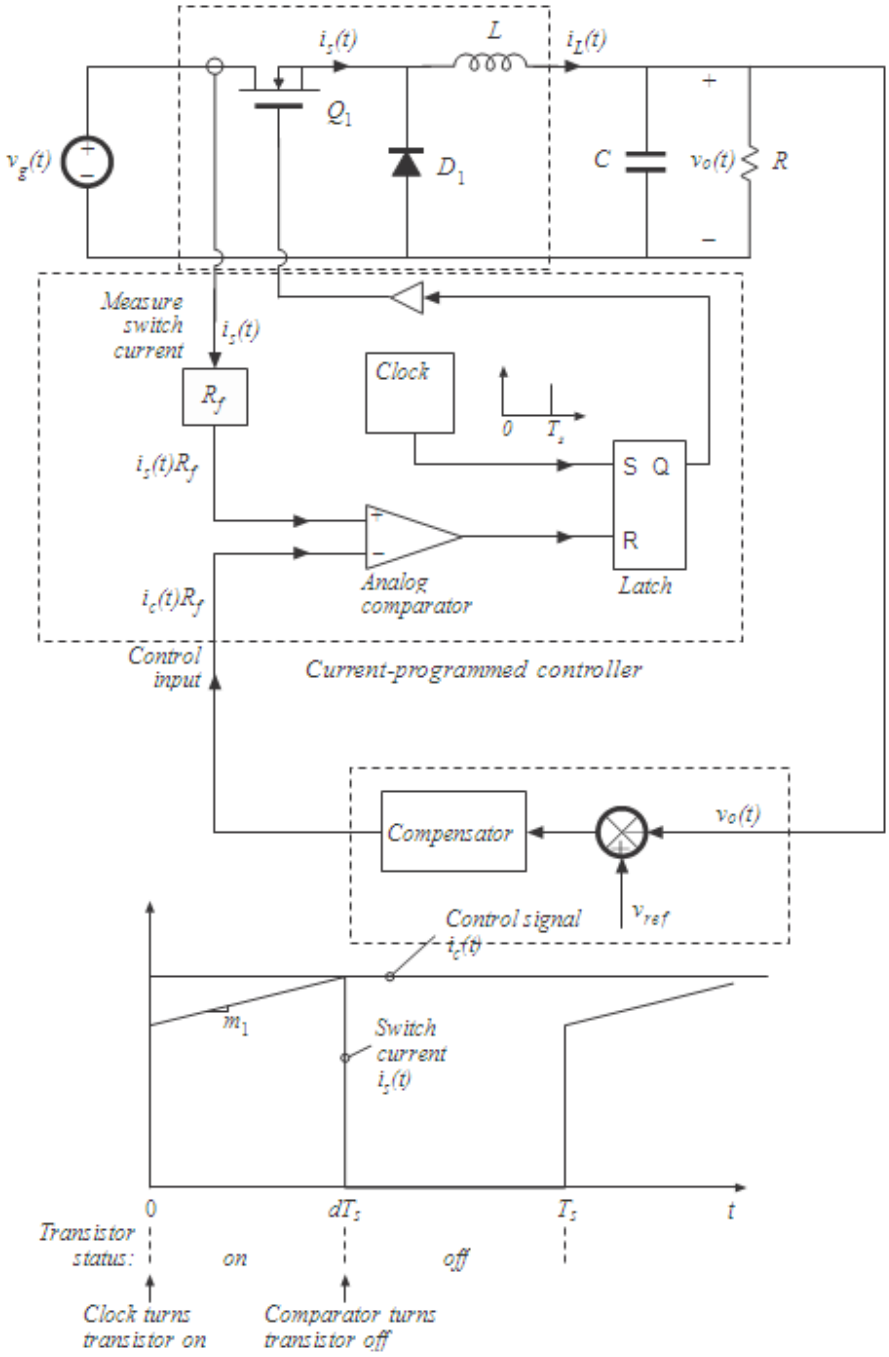
Current programmed control can be used to mitigate transformer saturation problems. Duty cycle control not recommended.



Ćuk isolated buck-derived converter

Capacitors C1a, C1b ensure that no dc voltage is applied to transformer primary or secondary windings. Transformer operates in conventional manner, with small magnetizing current and negligible energy storage within the magnetizing inductance.

9. Current programmed control principle (for a buck converter): block diagram, advantages, disadvantage, stability.



Advantages:

- ✓ Simpler dynamics —inductor pole is moved to high frequency.
- ✓ Simple robust output voltage control, with large phase margin, can be obtained without use of compensator lead networks.

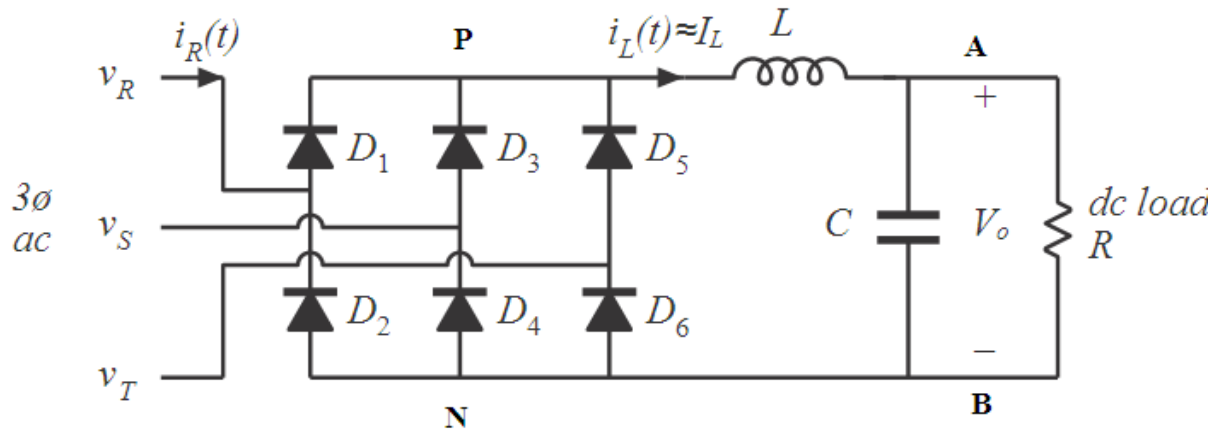
✓ Transistor failures due to excessive current can be prevented simply by limiting $i_c(t)$.

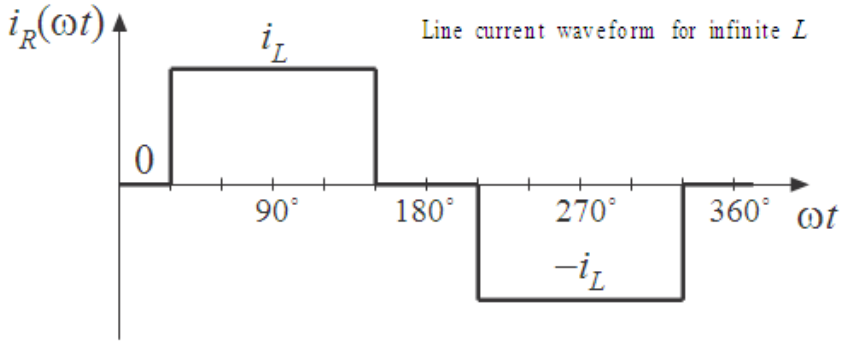
✓ Transformer saturation problems in bridge or push-pull converters can be mitigated.

Disadvantage: susceptibility to noise, instability problems.

The current programmed controller is inherently unstable for $D > 0.5$, regardless of the converter topology. Controller can be stabilized by addition of an artificial ramp.

10. The three-phase bridge rectifier (six pulse rectifier): schematics, line current for high load inductor, harmonic content of the line current and output voltage.





✓ Dc and a fundamental of *six* times the line frequency in the output voltage. That is the harmonics, relative to line frequency are: 0, 6, 12, 18, etc.

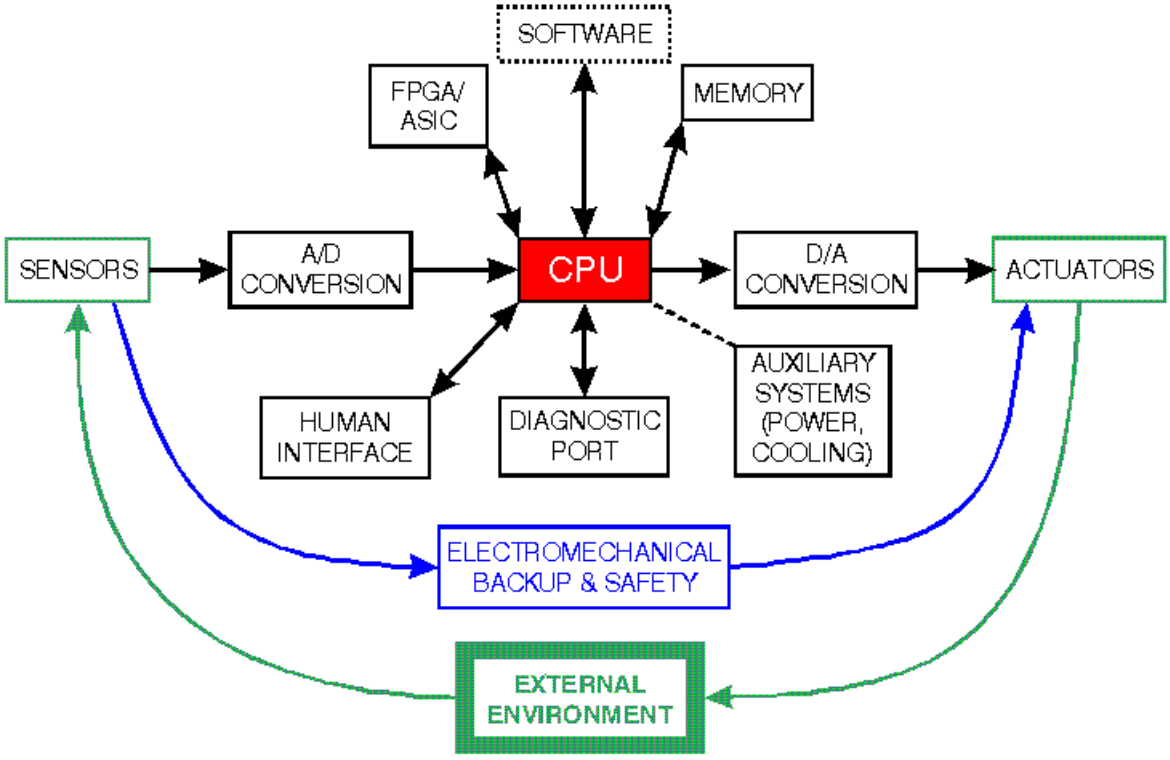
✓ Odd non-triplen harmonics in the ac line current.

Embedded Systems

1. *The general architecture of an embedded system.*

Answer: C.-D. Căleanu, Embedded Systems. Course Notes, 2011

https://intranet.etc.upt.ro/~EMBEDDED_SYS/Course , CHAPTER 1 slide 21.



2. *What are the relative advantages/disadvantages of RISC versus CISC architectures?*

Answer: C.-D. Căleanu, Embedded Systems. Course Notes, 2011

https://intranet.etc.upt.ro/~EMBEDDED_SYS/Course , CHAPTER 3, slides 13-15.

- The most common types of general-purpose ISA architectures implemented in embedded processors are:
- Complex Instruction Set Computing (CISC) Model
- Reduced Instruction Set Computing (RISC) Model

Complex Instruction Set Computing (CISC) Characteristics:

- A large number of instructions each carrying out different permutation of the same operation
- Instructions provide for complex operations
- Different instructions of different format
- Different instructions of different length
- Different addressing modes
- Requires multiple cycles for execution

Reduced Instruction Set Computing (RISC) Characteristics:

- Fewer instructions aiming simple operations that can be executed in a single cycle
- Each instruction of fixed length – facilitates instruction pipelining
- Large general purpose register set – can contain data or address
- Load-store Architecture – no memory access for data processing instructions

3. Enounce and explain the role of the following ARM registers: r13, r14 and r15, status registers.

Answer: C.-D. Căleanu, Embedded Systems. Course Notes, 2011

https://intranet.etc.upt.ro/~EMBEDDED_SYS/Course , CHAPTER 4, slide 17, 21

Three registers r13, r14, r15 perform special functions:

r13 – stack pointer,

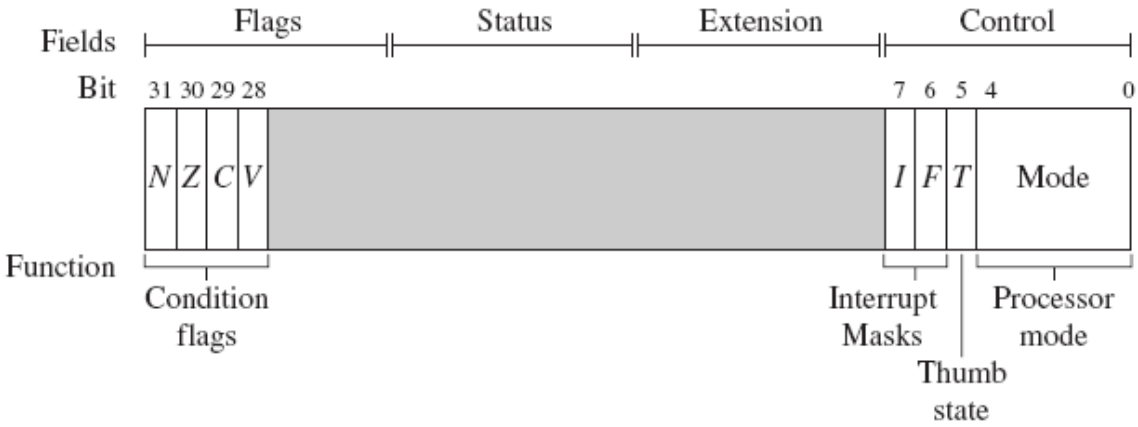
r14 – link register where return address is put whenever a subroutine is called,

r15 – program counter

In addition, there are two status registers

- CPSR: current program status register
- SPSR: saved program status register

CPSR: monitors and control internal operations



The top four bits of the CPSR contain the condition codes which are set by the CPU. The condition codes report the result status of a data processing operation. From the condition codes you can tell if a data processing instruction generated a negative, zero, carry or overflow result.

The lowest eight bits in the CPSR contain flags which may be set or clear ed by the application code. Bits 7 and 8 are the I and F bits. These bits are used to enable and disable the two interrupt sources which are external to the ARM7 CPU. Most peripherals are connected to these two interrupt lines. You should be careful when programming these two bits because in order to disable either interrupt source the bit must be set to '1' not '0' as you might expect. Bit 5 is the THUMB bit.

4. *Which is the role of the barrel shifter? Present its block diagram and enumerate the basic operations which could be performed with it. Illustrate the concept with an assembly language example.*

Answer: C.-D. Căleanu, Embedded Systems. Course Notes, 2011

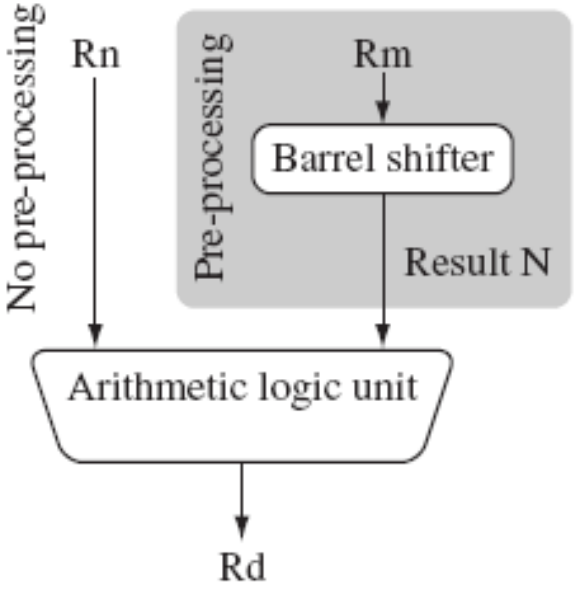
https://intranet.etc.upt.ro/~EMBEDDED_SYS/Course , CHAPTER 4, slide 43, 44.

Enables shifting 32-bit operand in one of the source registers left or right by a specific number of positions within the cycle time of instruction

Basic Barrel shifter operations: Shift left, right, rotate

Facilitates fast multiply, division and increases code density

Example: mov r7, r5, LSL #2 - Multiplies content of r5 by 4 and puts result in r7



5. Present possible implementations for the non-volatile memory. What could be store in it?

Answer: C.-D. Căleanu, Embedded Systems. Course Notes, 2011

https://intranet.etc.upt.ro/~EMBEDDED_SYS/Course , CHAPTER 5, slide 10-12.

- Mask ROM
  - Used for dedicated functionality
  - Contents fixed at IC fab time (truly write once!)
- ERPOM (erase programmable)
  - Requires special IC process (floating gate technology)
  - Writing is slower than RAM, EPROM uses special programming system to provide special voltages and timing
  - Reading can be made fairly fast
  - Rewriting is slow
    - Erasure is first required, EPROM – UV light exposure, EEPROM – electrically erasable
- Flash
  - Uses single transistor per bit (EEPROM employs two transistors)
  - A flash memory provides high density storage with speed marginally less than that of SRAM's
  - Write time is significantly higher compared to DRAM