It could be shown that knowing f_{0dB} is sufficient for computing f_d:

$$f_d = f_{0dB}\left|\frac{A_f}{A_0}\right|$$

where A_0 is the open-loop midband frequency gain.

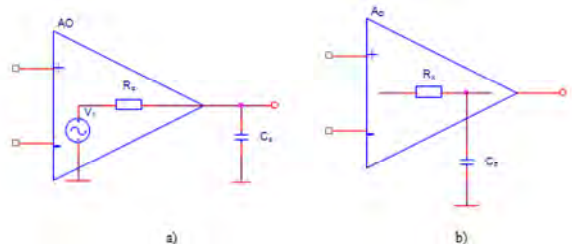

Fig. 5. Dominant-pole implementation.

10. Draw and characterize a Wien network and show how is connected to build a Wien oscillator. What are the conditions used to design feedback loops.

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2011 Sem 7.ppt

3.2 The Wien Bridge Oscillator

An oscillator circuit in which a balanced bridge is used as the feedback network

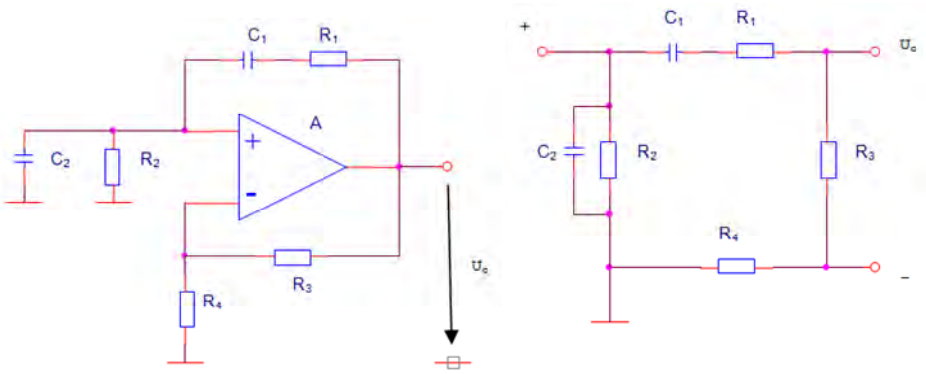


Fig. 4. a) A Wien bridge oscillator. b) The bridge network

Barkhausen Criterion.

- The condition for the feedback loop to provide sinusoidal oscillation of frequency ω is:

$$A(j\omega)\beta(j\omega) = 1 \Leftrightarrow$$

$$\begin{cases} \arg A(j\omega) + \arg \beta(j\omega) = 2k\pi & \text{phase criterion} \\ \left|A(j\omega)\right|\left|\beta(j\omega)\right| = 1 & \text{amplitude criterion.} \end{cases}$$

Amplitude criterion. $$\left|\underline{A}_{ur}\right|\left|\underline{\beta}_{+}\right|_{\omega=\omega_0} = 1$$

For negative feedback loop: $$\underline{A}_{ur} = \frac{A_u}{1+\beta_- A_u} \cong \frac{1}{\beta_-}$$

=> $$\left|\underline{\beta}_{+}\right| = \left|\underline{\beta}_{-}\right|$$

$$\beta_- = \frac{R_4}{R_3 + R_4}$$

$$\beta_+(j\omega) = \frac{1}{1 + \frac{R_1}{R_2} + \frac{C_2}{C_1} + j\left(\omega C_2 R_1 - \frac{1}{\omega C_1 R_2}\right)}$$

In order to obtain oscillations, **phase criterion** has to be satisfied:

$$\beta_+(j\omega_0) \in \Re \Rightarrow \omega_0 C_2 R_1 - \frac{1}{\omega_0 C_1 R_2} = 0;$$

$$\omega_0^2 = \frac{1}{R_1 C_1 R_2 C_2} \Rightarrow f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}}$$

$$\begin{cases} \arg\left[\beta_+(j\omega_0)\right] = 0 \\ \left|\beta_+(j\omega_0)\right| = \dfrac{1}{1 + \dfrac{R_1}{R_2} + \dfrac{C_2}{C_1}} \end{cases}$$

Digital Integrated Circuits

1. *Positive edge triggered D type flip-flop: draw a symbolic representation, the operating table and its associated waveforms*

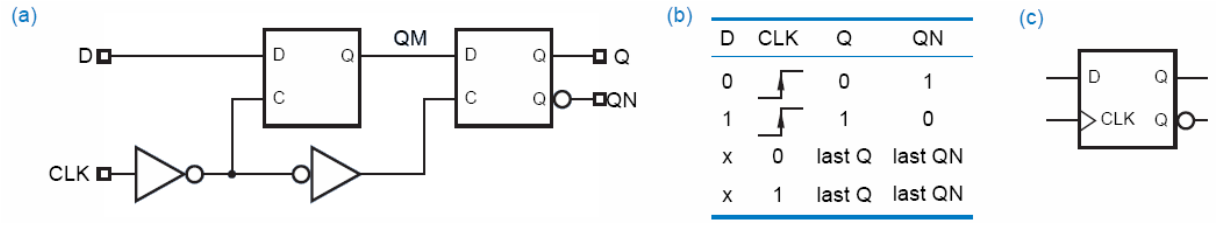
A positive-edge-triggered D flip-flop combines a pair of D latches, to create a circuit that samples its D input and changes its Q and QN outputs only at the rising edge of a controlling CLK signal.

The first latch is called the master; it is open and follows the input when CLK is 0. When CLK goes to 1, the master latch is closed and its output is transferred to the second latch, called the slave.

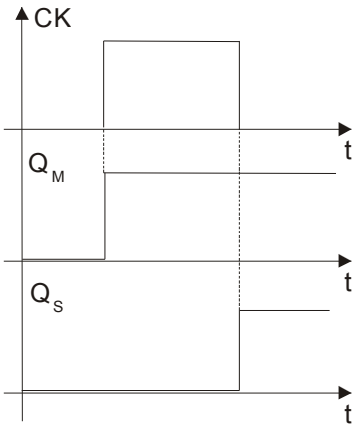
The slave latch is open all the while that CLK is 1, but changes only at the beginning of this interval, because the master is closed and unchanging during the rest of the interval.

Edge-Triggered D Flip-Flop

The triangle on the D flip-flop's CLK input indicates edge-triggered behavior, and is called a *dynamic-input indicator*.

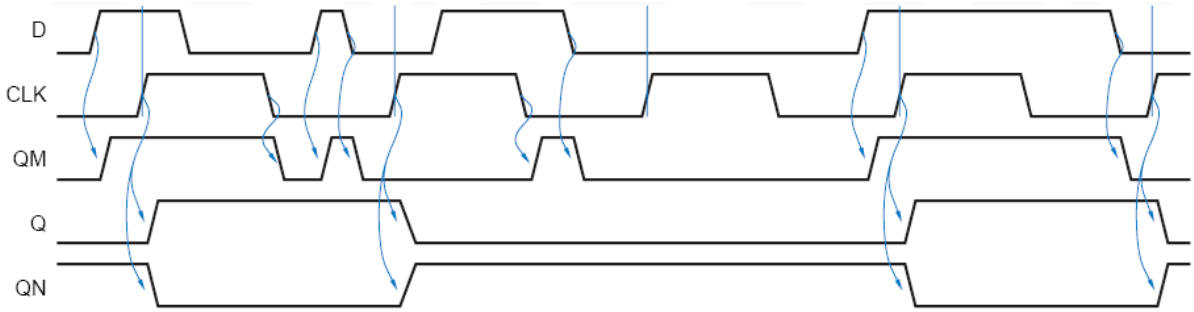


D	CLK	Q	QN
0	↑	0	1
1	↑	1	0
x	0	last Q	last QN
x	1	last Q	last QN

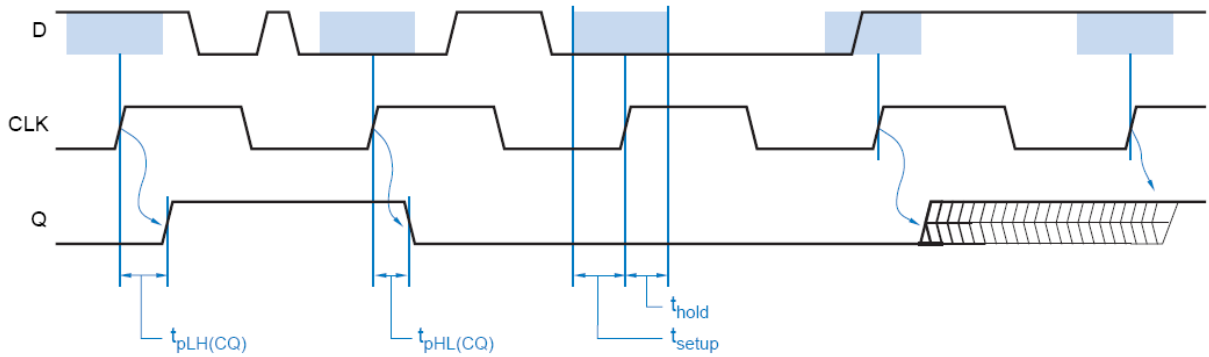


The QM signal shown is the output of the master latch.

Notice that QM changes only when CLK is 0. When CLK goes to 1, the current value of QM is transferred to Q, and QM is prevented from changing until CLK goes to 0 again.



Like a D latch, the edge-triggered D flip-flop has a setup and hold time window during which the D inputs must not change. This window occurs around the triggering edge of CLK, and is indicated by shaded color.



2. *Explain how a decoder can be used as a demultiplexer*

The 74x138 is a commercially available MSI 3-to-8 decoder whose gate-level circuit diagram and symbol are shown in Figure 5-37; its truth table is given in Table 5-7.

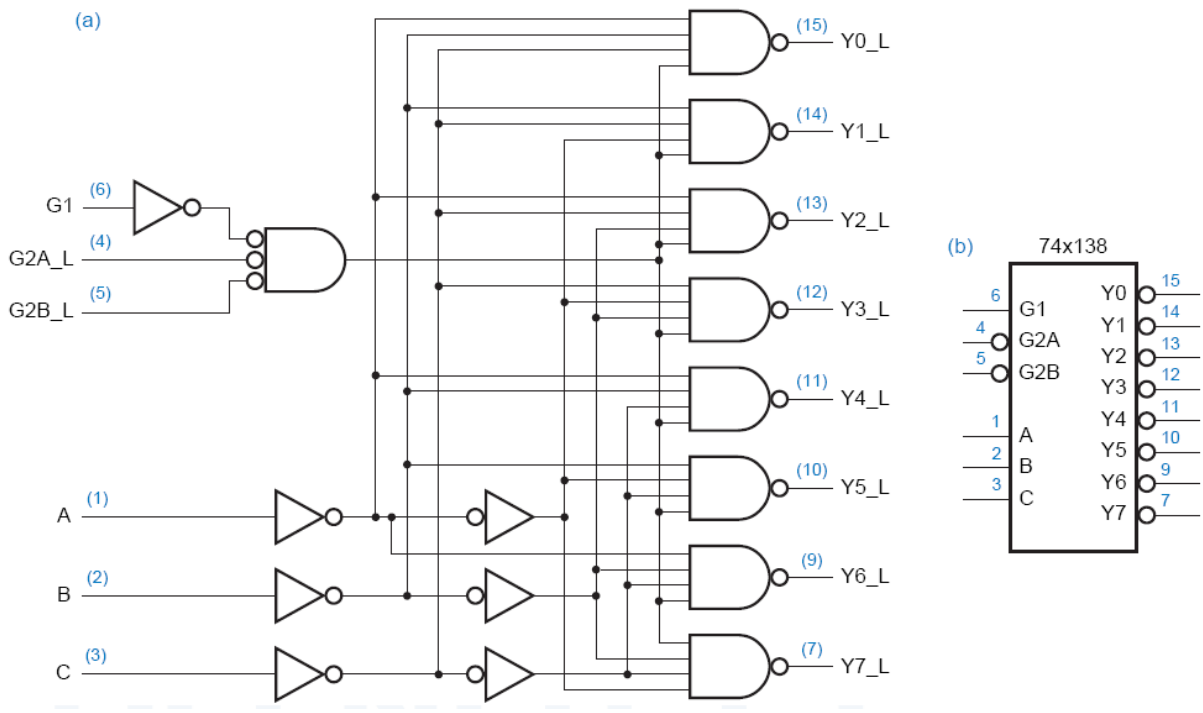


Figure 5-37

Like the 74x139, the 74x138 has active-low outputs, and it has three enable inputs (G1, nG2A, nG2B), all of which must be asserted for the selected output to be asserted.

Thus, we can easily write logic equations for an internal output signal such as Y5 in terms of the internal input signals:

However, because of the inversion bubbles, we have the following relations between internal and external signals:

Y5 = G1.G2A.G2B . C . nB . A

Enable Select

Therefore, if we're interested, we can write the following equation for the external output signal Y5_L in terms of external input signals:

G2A = nG2A_nL

G2B = nG2B_nL

Y5 = nY5_nL

Y5_L = nY5 = n(G1 . nG2A_nL . nG2B_nL . C . nB . A)

= nG1 + G2A_L + G2B_L + nC + B + nA

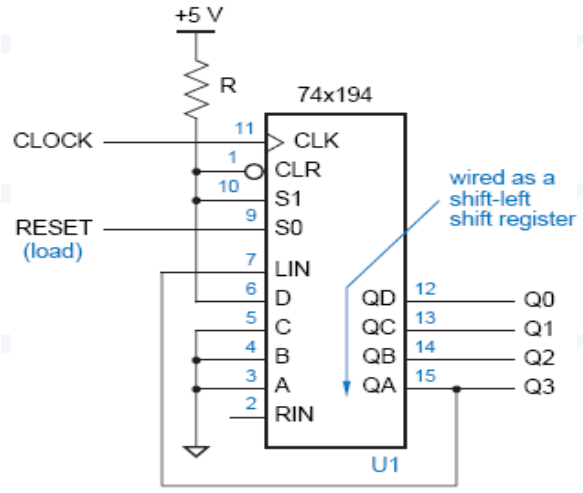
Table 5-7

74x138 – Truth Table

Inputs						Outputs							
G1	nG2a	nG2b	C	B	A	nY7	nY6	nY5	nY4	nY3	nY2	nY1	nY0
0	x	x	x	x	x	1	1	1	1	1	1	1	1
x	1	x	x	x	x	1	1	1	1	1	1	1	1
x	x	1	x	x	x	1	1	1	1	1	1	1	1
1	0	0	0	0	0	1	1	1	1	1	1	1	0
1	0	0	0	0	1	1	1	1	1	1	1	0	1
1	0	0	0	1	0	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	0	1	1	1
1	0	0	1	0	0	1	1	1	0	1	1	1	1
1	0	0	1	0	1	1	1	0	1	1	1	1	1
1	0	0	1	1	0	1	0	1	1	1	1	1	1
1	0	0	1	1	1	0	1	1	1	1	1	1	1

3. *4 bit Ring counter: schematic, explain its operation, main waveforms*

The simplest shift-register counter uses an n-bit shift register to obtain a counter with n states, and is called a ring counter. Figure shows the logic diagram for a 4-bit ring counter.

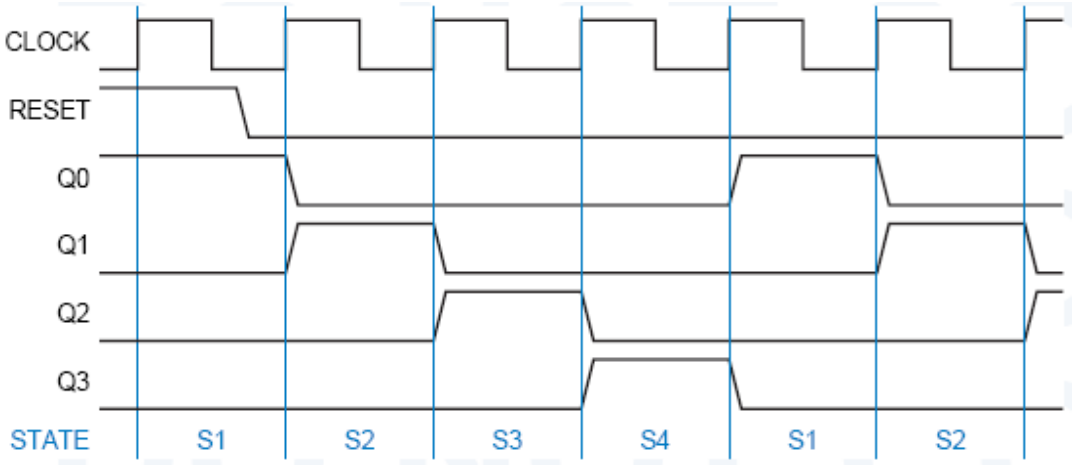


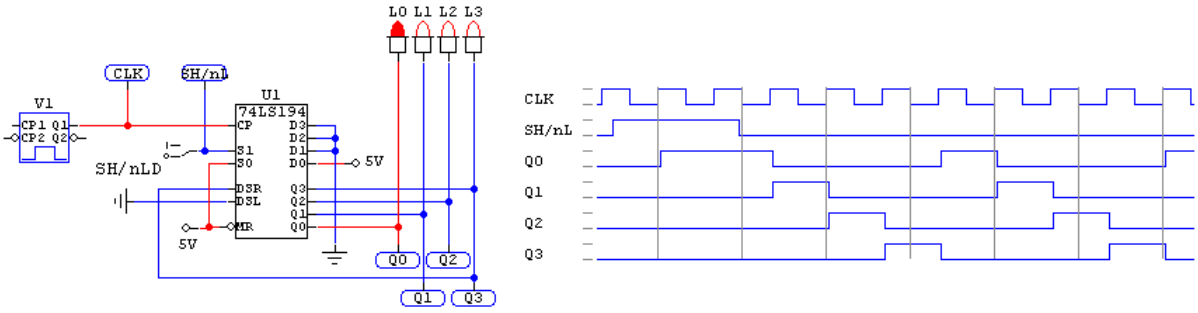
The 74x194 universal shift register is wired so that it normally performs a left shift. However, when RESET is asserted, it loads 0001 (refer to the '194's function table).

Once RESET is negated, the ’194 shifts left on each clock tick. The LIN serial input is connected to the “leftmost” output, so the next states are 0010, 0100, 1000, 0001, 0010, ….

Thus, the counter visits four unique states before repeating.

A timing diagram is shown. An n-bit ring counter visits n states in a cycle.





Ring counter with 74LS194 and timing diagrams

	CLK	Q_0	Q_1	Q_2	Q_3	**Explicaţie**
Initializare	0	0	0	0	0	nMR = 0
	1	1	0	0	0	S1 S0 = 11 (parallel load)
Complete cycle: 4 CLKs	2	0	1	0	0	S1 S0 = 01 (shift right)
	3	0	0	1	0	
	4	0	0	0	1	
	5 (1)	1	0	0	0	

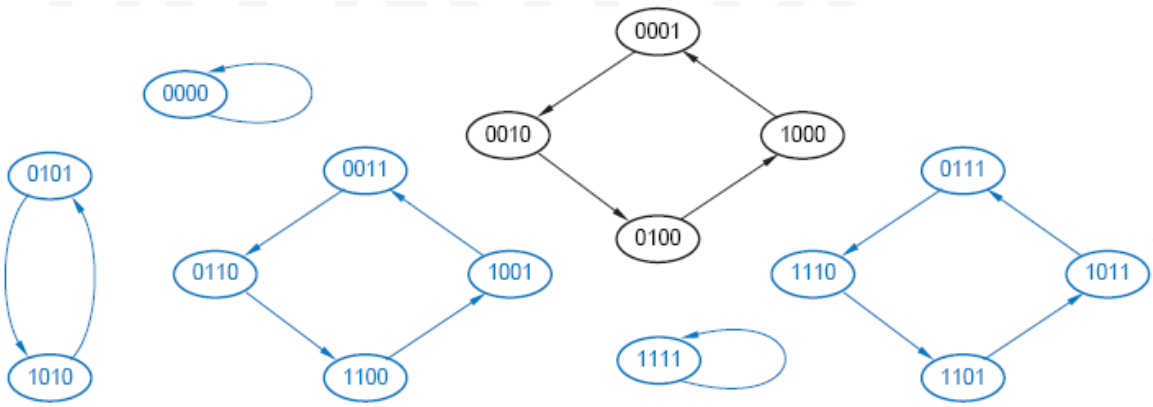
The ring counter already introduced has one major problem—it is not robust.

If its single 1 output is lost due to a temporary hardware problem (e.g., noise), the counter goes to state 0000 and stays there forever.

Likewise, if an extra 1 output is set (i.e., state 0101 is created), the counter will go through an incorrect cycle of states and stay in that cycle forever.

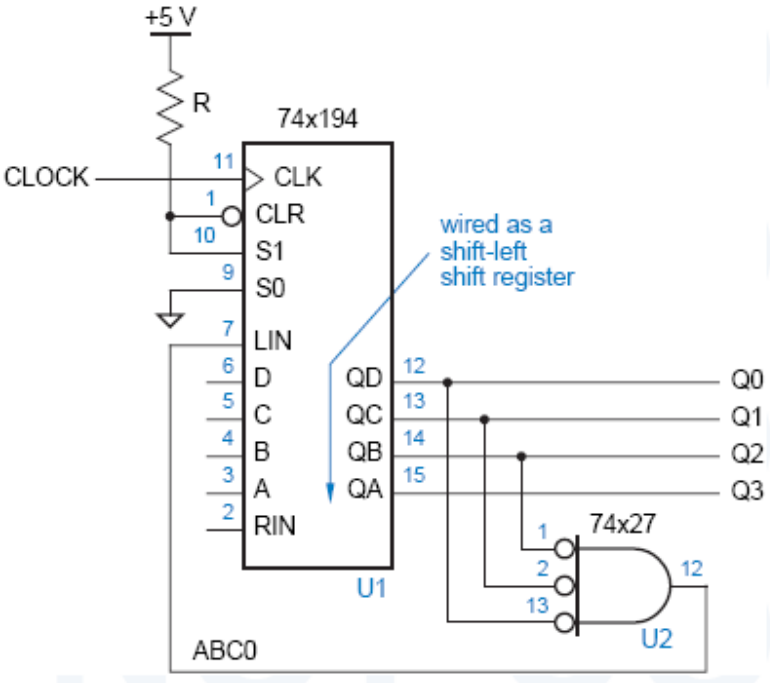
These problems are quite evident if we draw the complete state diagram for the counter circuit, which has 16 states.

As shown, there are 12 states that are not part of the normal counting cycle. If the counter somehow gets off the normal cycle, it stays off it.



4. *Self correcting counters built around registers. Give at least 2 examples: schematic, explain its operation, main waveforms*

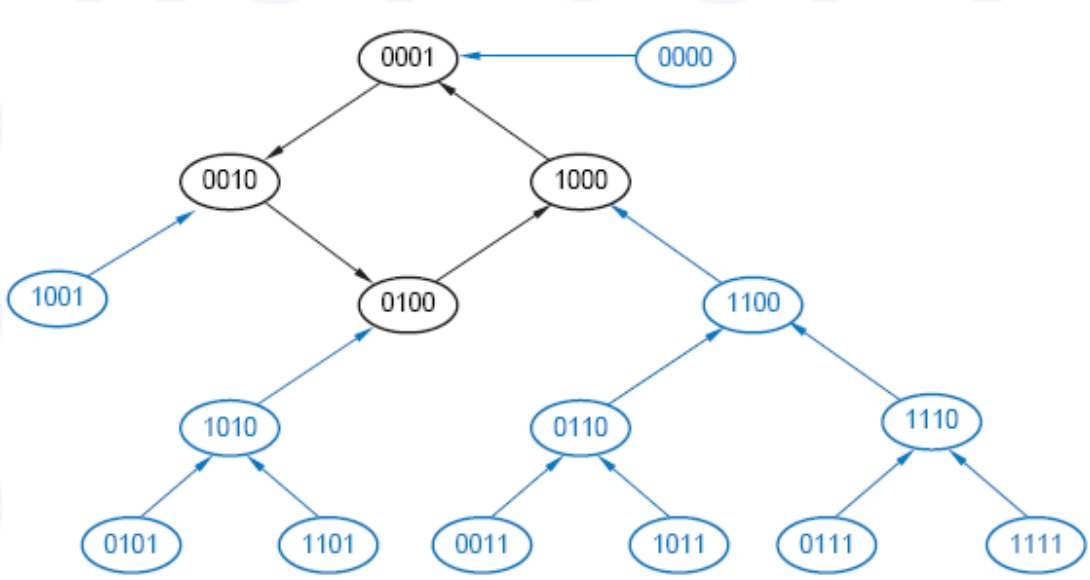
A self-correcting ring counter circuit is shown. The circuit uses a NOR gate to shift a 1 into LIN only when the three least significant bits are 0.



Notice that, in this circuit, an explicit RESET signal is not necessarily required. Regardless of the initial state of the shift register on power up, it reaches state 0001 within four clock ticks.

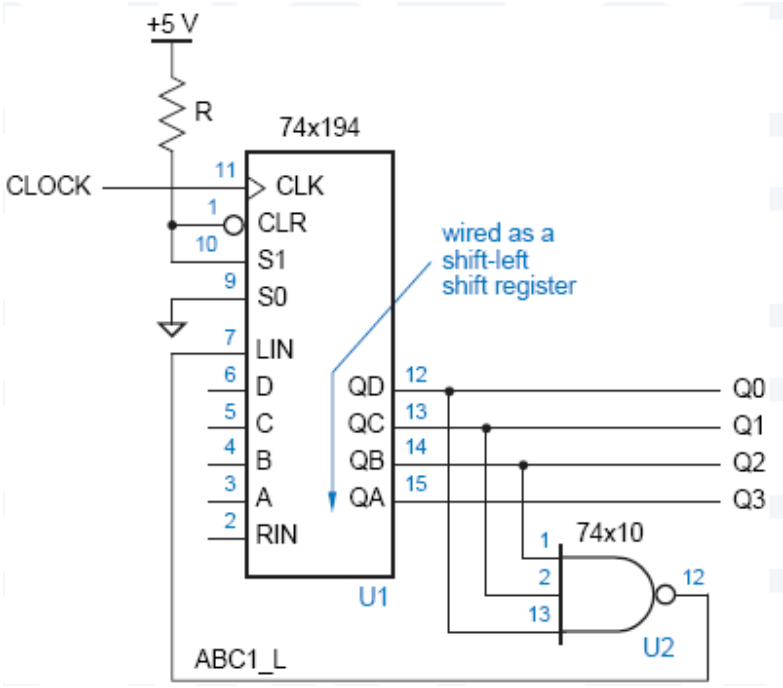
Therefore, an explicit reset signal is required only if it is necessary to ensure that the counter starts up synchronously with other devices in the system or to provide a known starting point in simulation.

This results in the state diagram; all abnormal states lead back into the normal cycle.



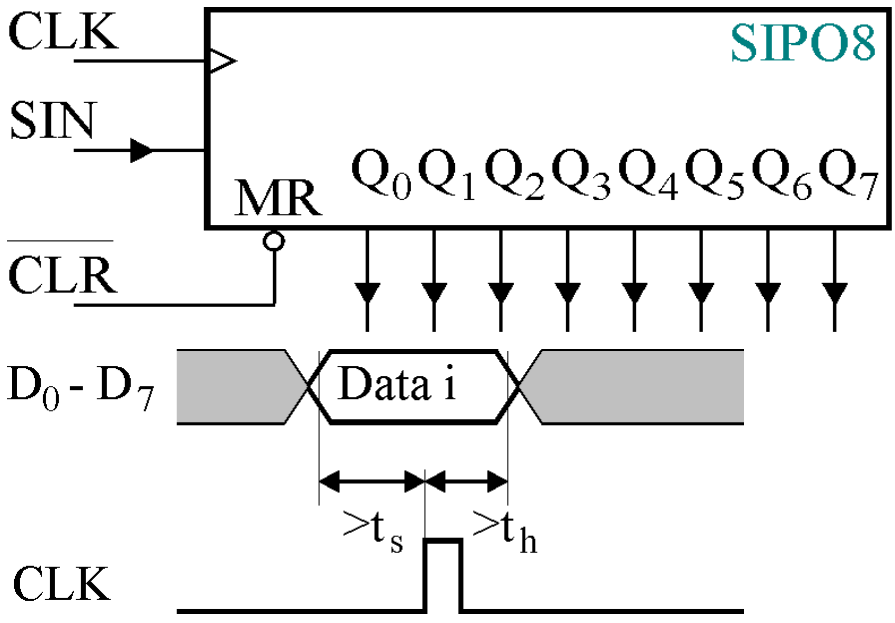
For the general case, an n-bit self-correcting ring counter uses an n-1-input NOR gate, and corrects an abnormal state within n - 1 clock ticks.

In CMOS and TTL logic families, wide NAND gates are generally easier to come by than NORs, so it may be more convenient to design a self-correcting ring counter as shown in figure. States in this counter's normal cycle have a single circulating 0.

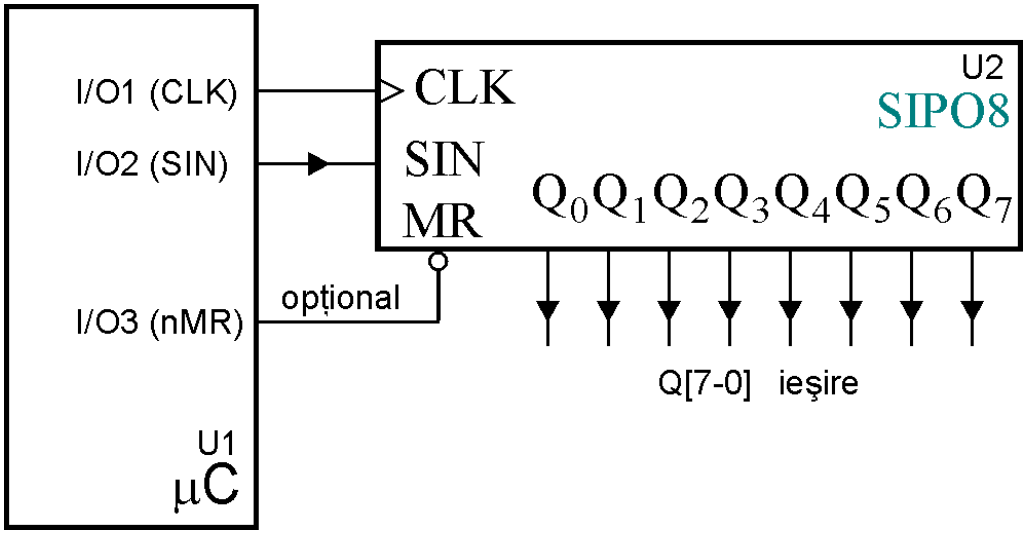


5. *Describe how to achieve parallel-to-serial, respectively serial-to-parallel data conversion*
Serial – parallel conversion

Uses a SIPO register:



Used for expanding the output pins for a low count pin microprocessor system
E.g. PIC16F84A has 18 pini, 13 are I/O
2 pins are used and extra 8 outputs are provided

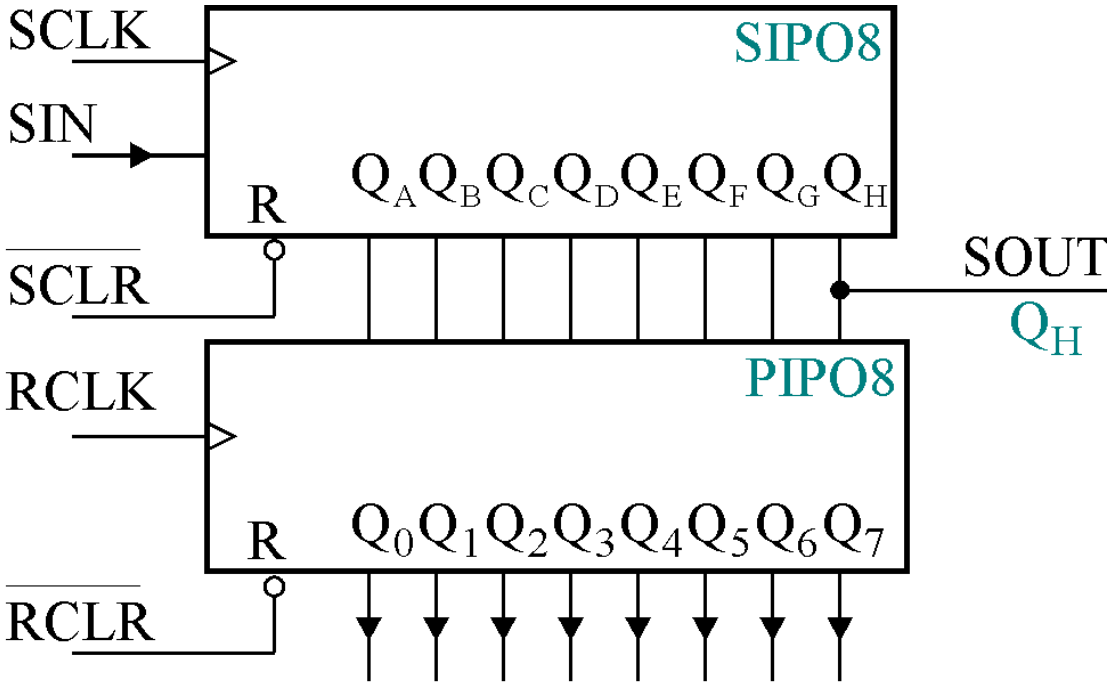


Expanding the output lines of a microcontroller

Serial – parallel conversion

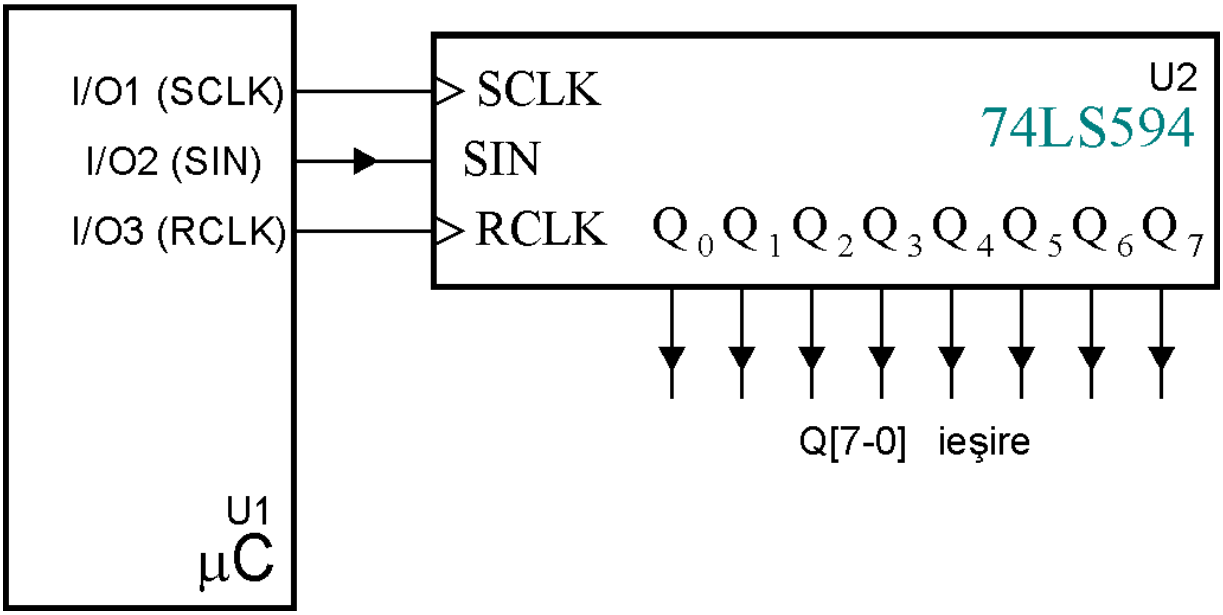
Problems when connecting fast devices

Solution: 74LS594 register



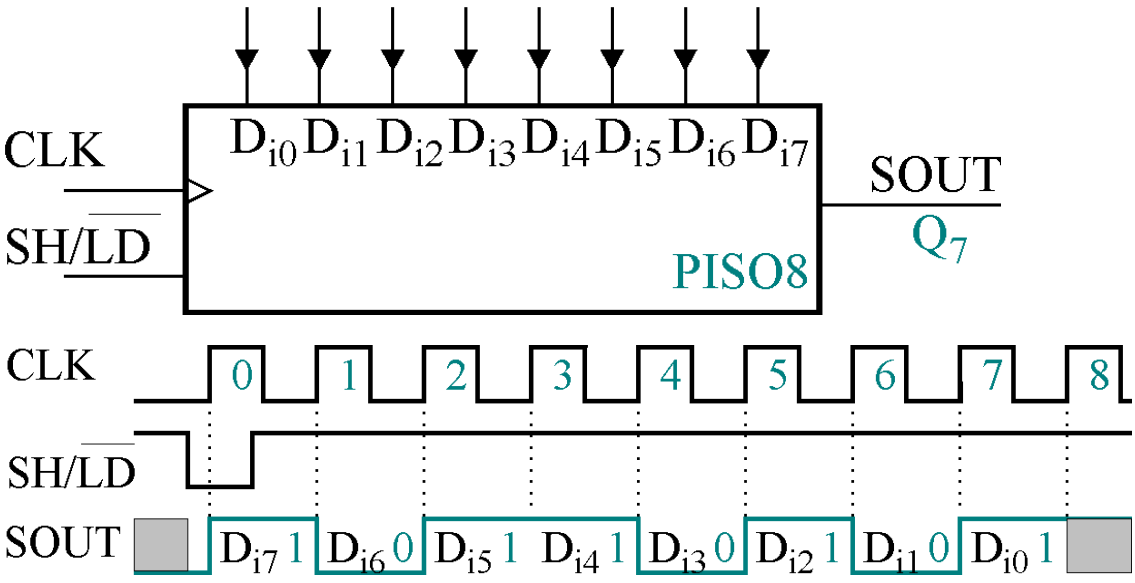
74LS594 – functional diagram

Serial – parallel conversion



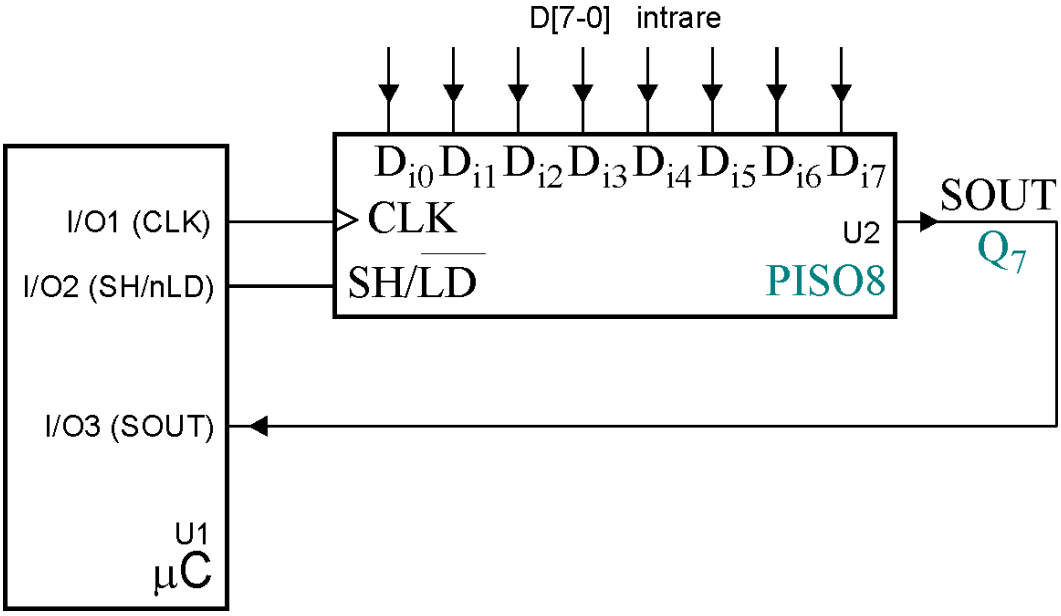
Expanding the Output lines of a microcontroller, 2nd version

Uses a PISO register:



Parallel – serial conversion

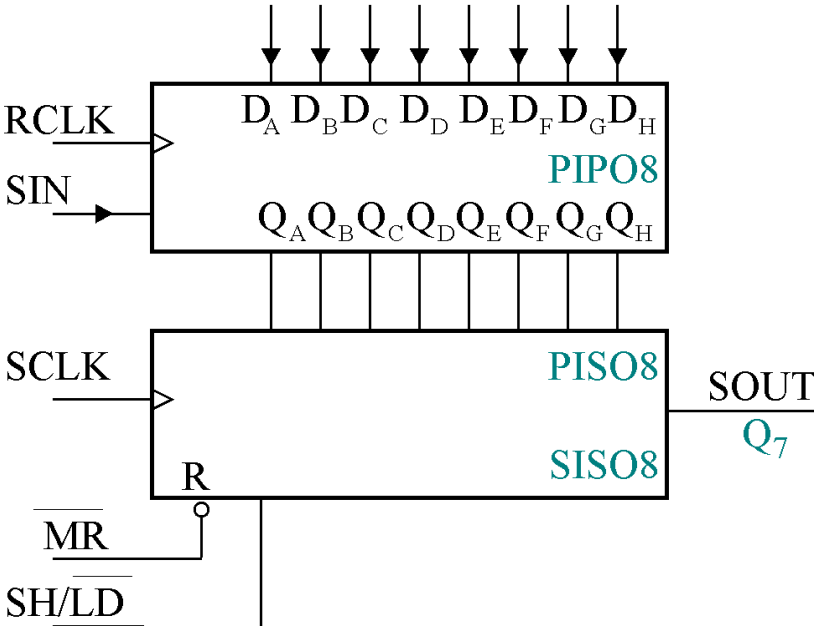
Parallel – serial conversion can be used to expand the input lines in a microcontroller system



Parallel – serial conversion

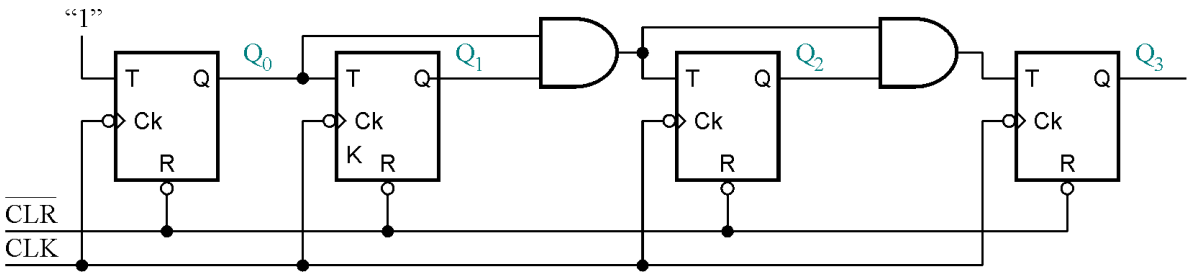
Same problem as before (with fast devices)

Solution: 74LS597 register



74LS597 – functional diagram

6. *4-bit binary synchronous counter. Draw the schematic diagram, explain its operation, and draw the relevant waveforms*

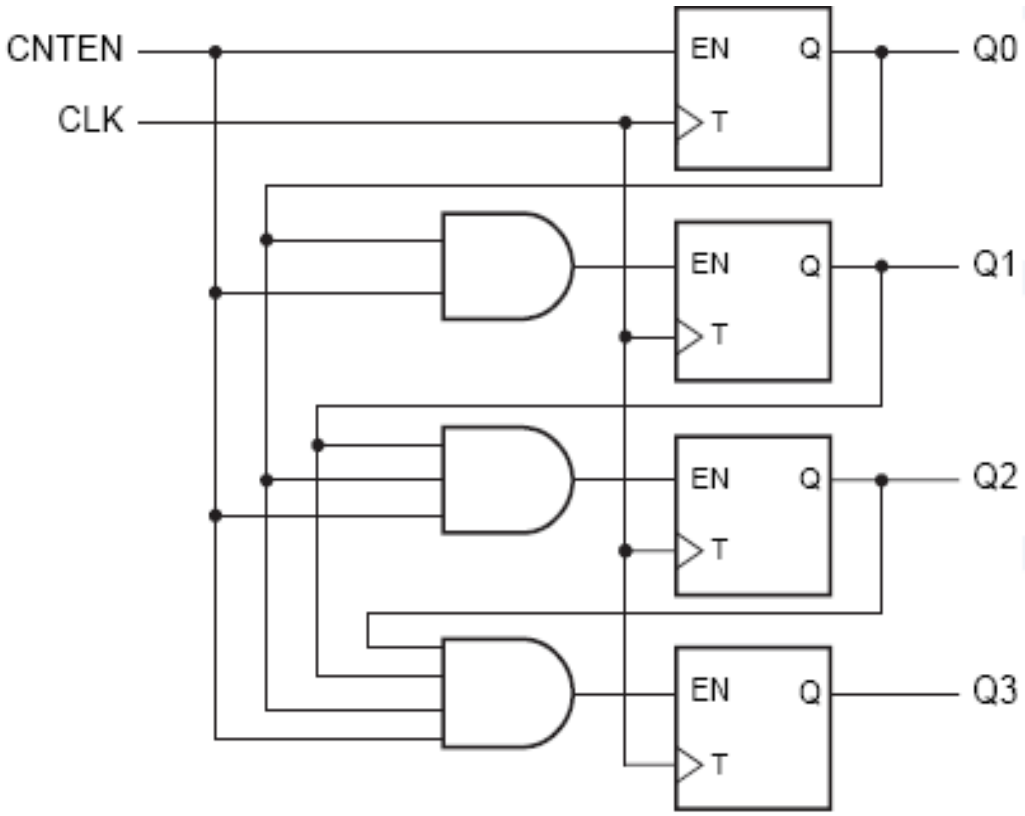


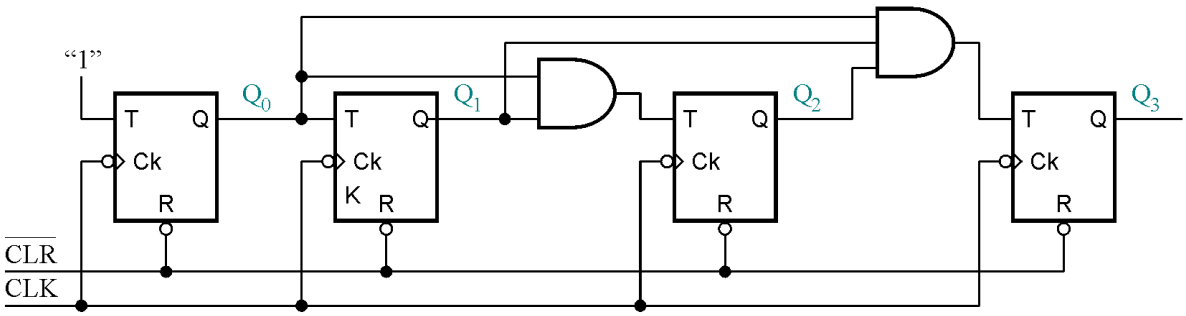
The counter structure previous presented is sometimes called a synchronous serial counter because the combinational enable signals propagate serially from the least significant to the most significant bits.

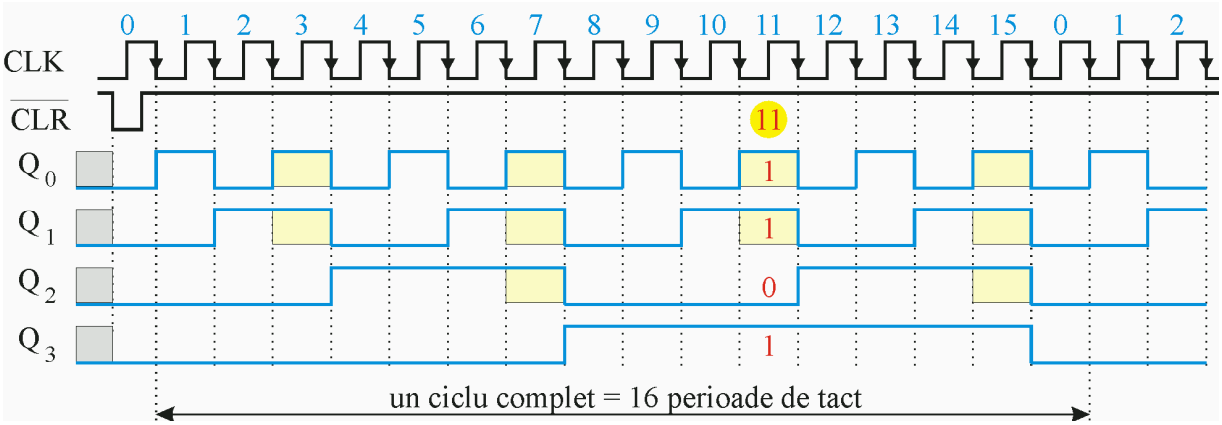
If the clock period is too short, there may not be enough time for a change in the counter's LSB to propagate to the MSB**.**

This problem is eliminated by driving each EN input with a dedicated AND gate, just a single level of logic.

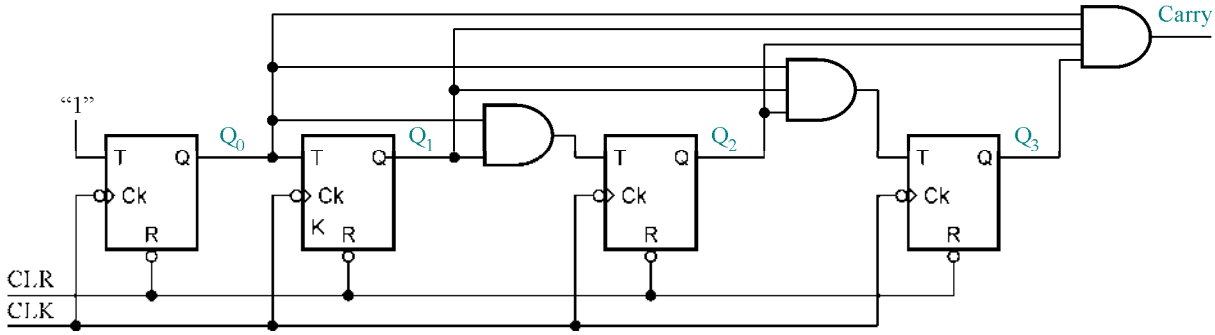
Called a synchronous parallel counter, this is the fastest binary counter structure**.**







Adding Output Carry Feature



7. Outline the main methods for obtaining modulus p frequency dividers and programmable frequency dividers

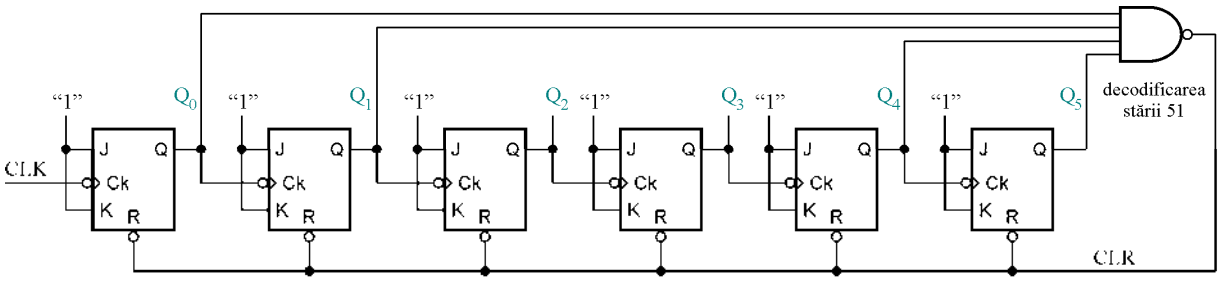
Modulus p Counter Design

Let p = 51

There are log251 = 6 flip flops needed

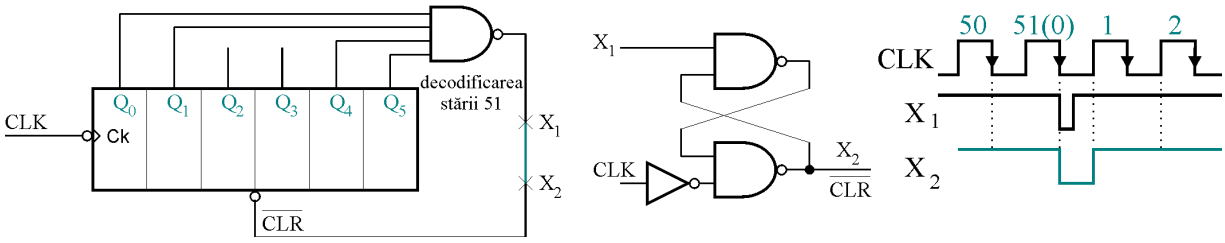
p = 51 = 1*32 + 1*16 + 0*8 + 0*4 +1*2 + 1*1

p = 1100112

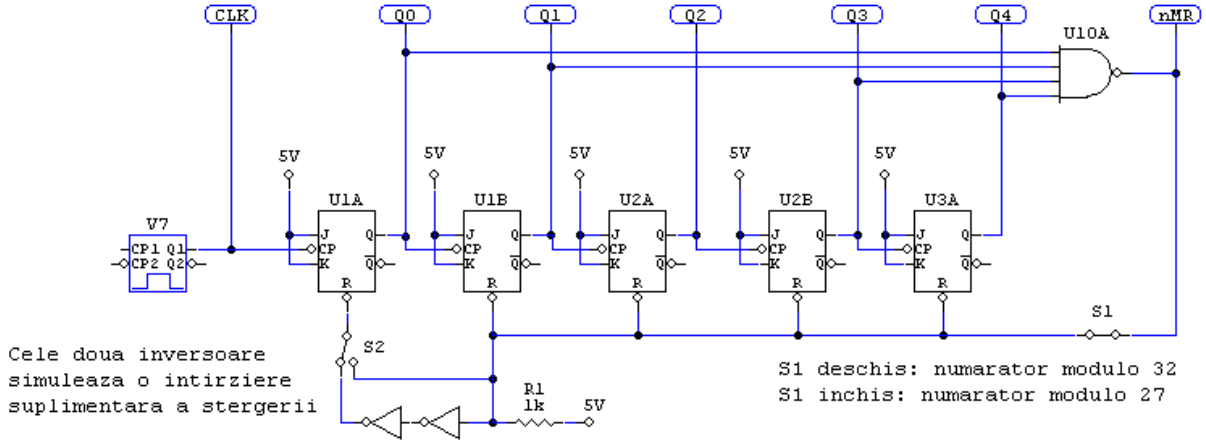


32	16	8	4	2	1
$Q_5 = 1$	$Q_4 = 1$	$Q_3 = 0$	$Q_2 = 0$	$Q_1 = 1$	$Q_0 = 1$

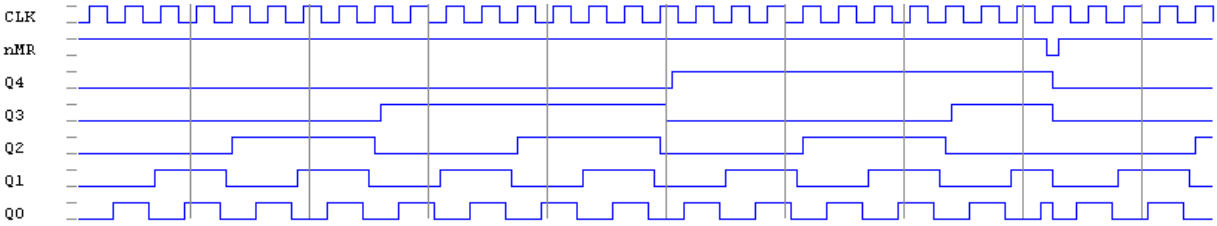
A latch to store the internal nCLR signal is needed



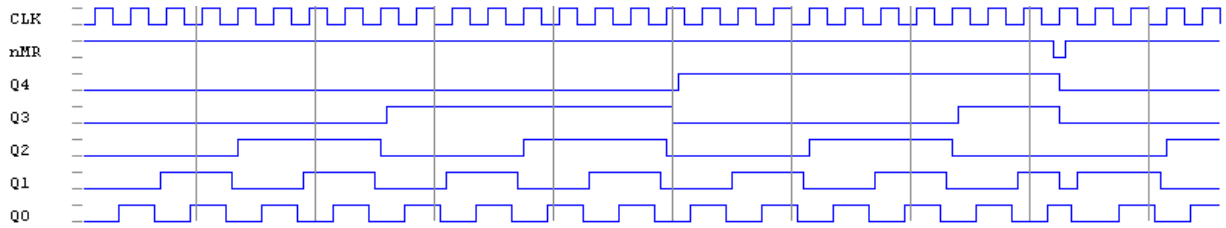
Simulation for p = 27



Ripple counter (p = 27) – simulated delayed Reset signal

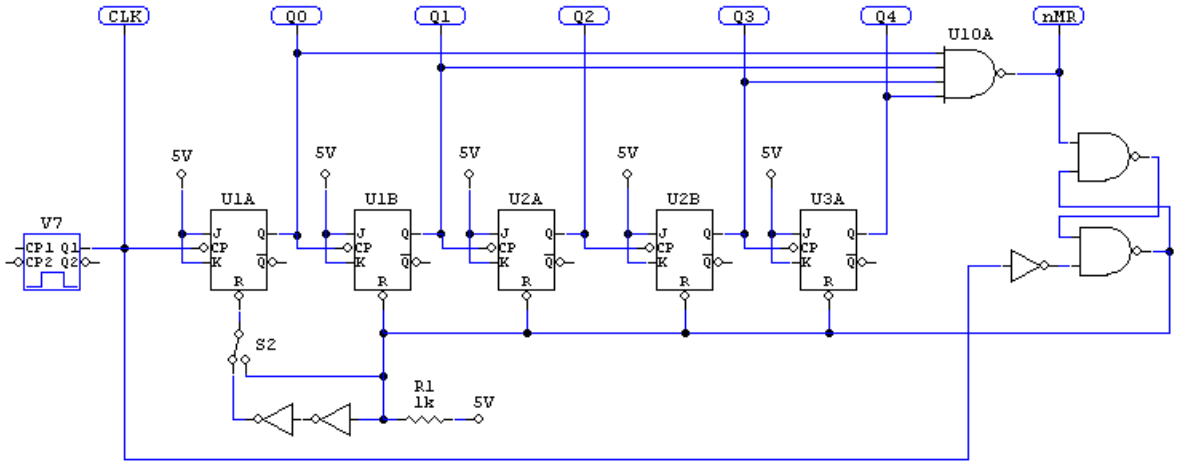


Modulus 27 counter, correct timing (S1 ON, S2 – to right)

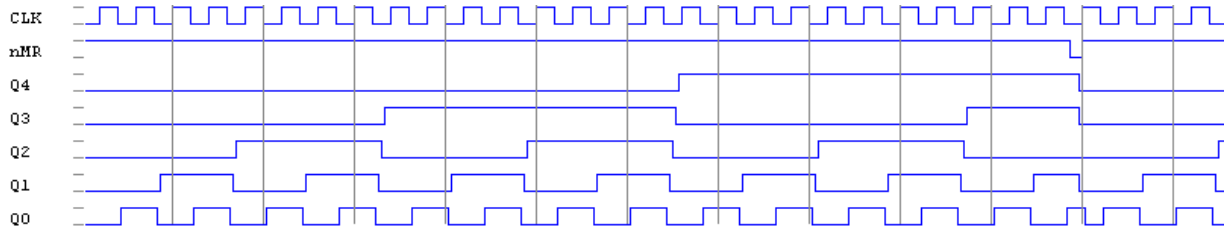


Modulus 27 counter, incorrect timing (S1 ON, S2 – to left) Sequence is ...26, 27+ CLR, 2, 3, ...

Adding the SR Latch



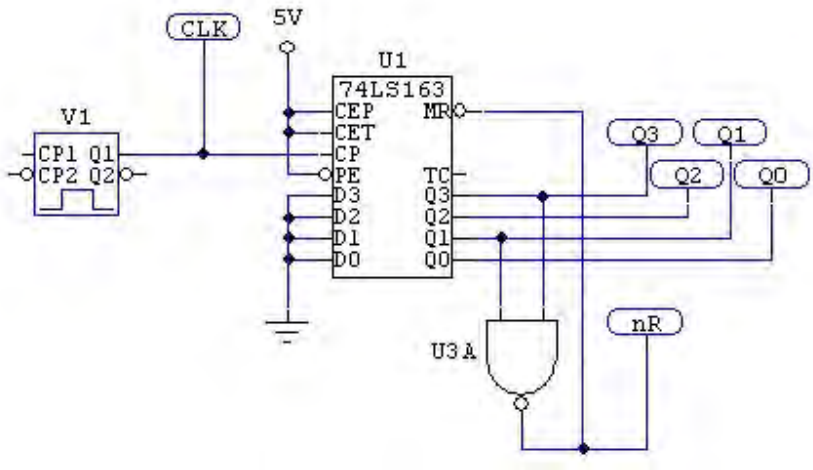
Correct timing



S1 ON, S2 to left

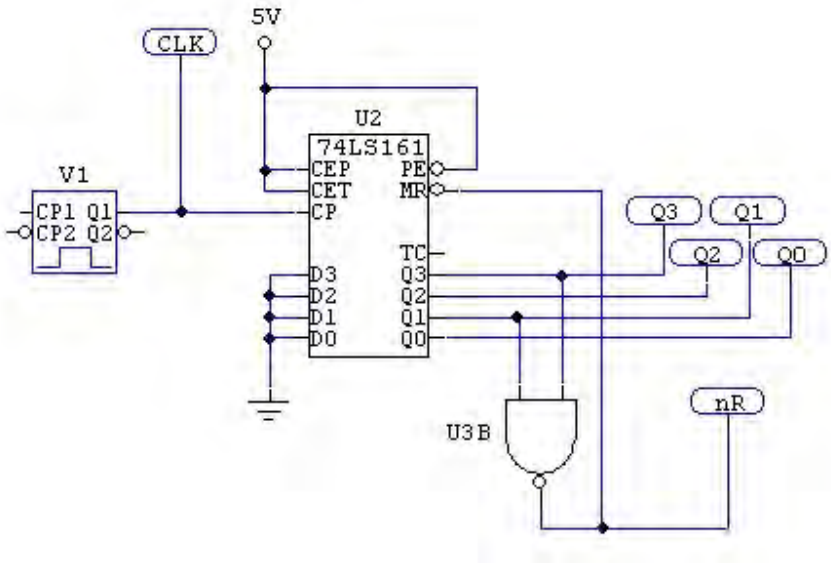
8. *Influence of Sync / Async Reset (explain using waveforms and a 74x163 based counter.*

Influence of Sync / Async Reset



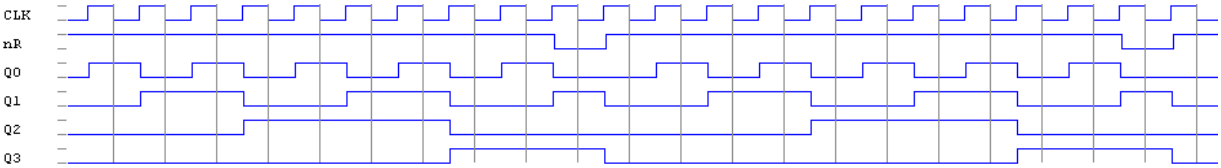
74x163 - Synchronous Reset

Modulus = 11

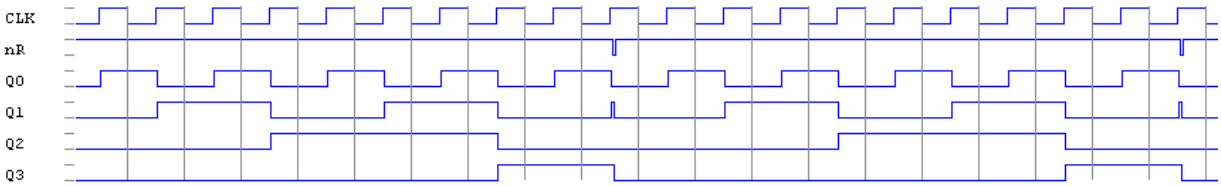


74x161 - Asynchronous Reset

Modulus = 10



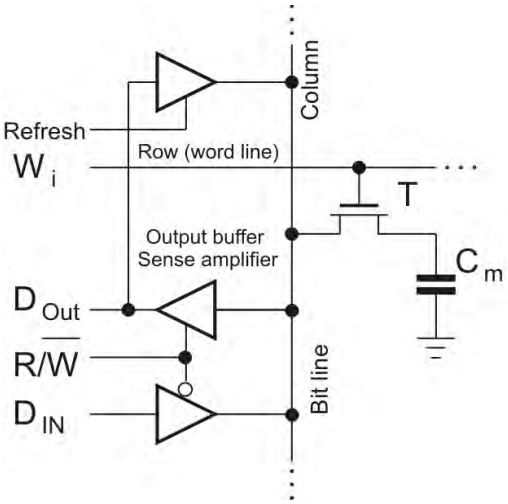
74x163 - Synchronous Reset – Modulus = 11



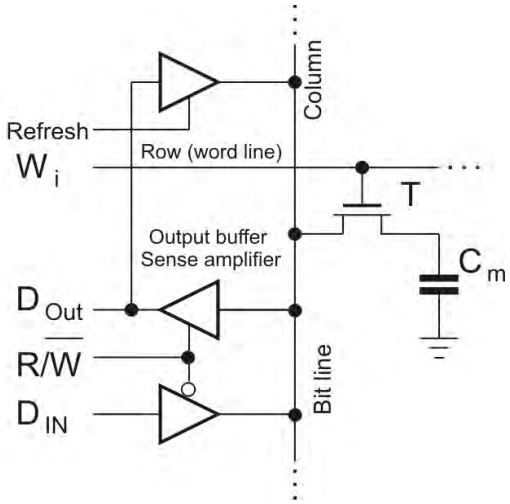
74x161 - Asynchronous Reset – Modulus = 10

9. *Explain briefly the operation of a DRAM - reading, writing, refresh*

DRAM – Write Operation

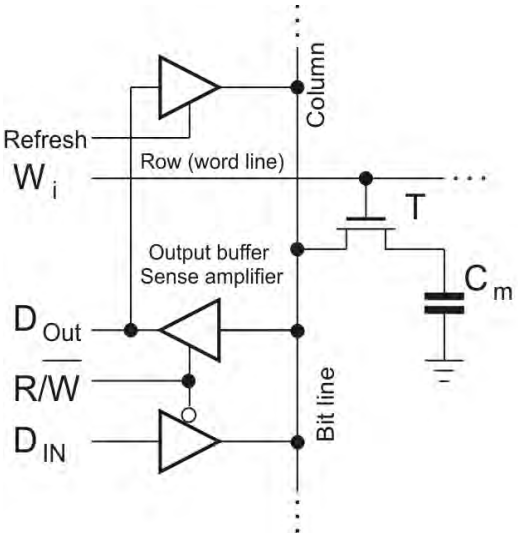


Writing a 1 into the memory cell

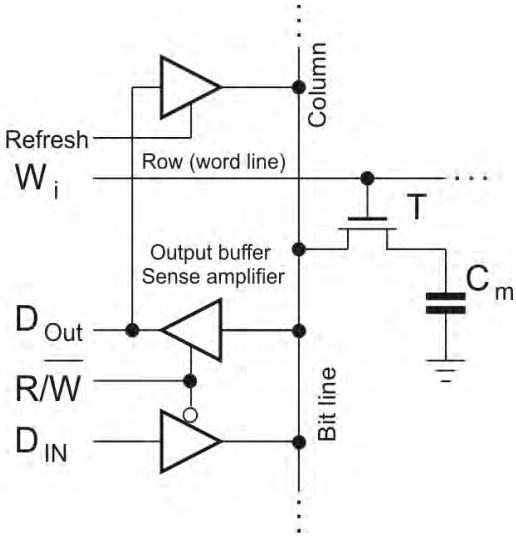


Writing a 0 into the memory cell

DRAM – Read Operation

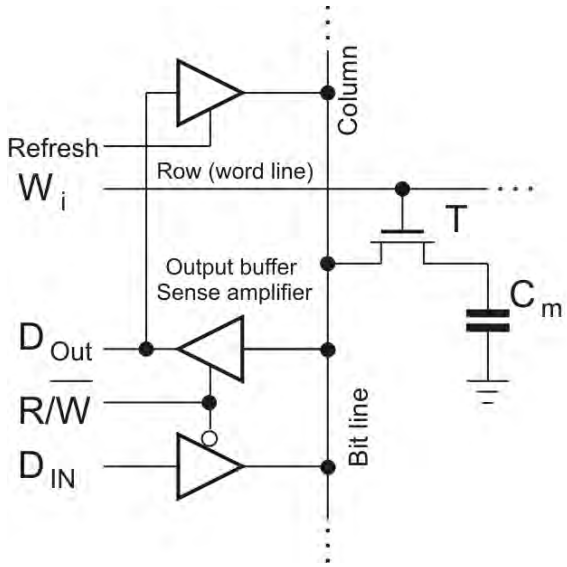


Reading a 1 from the memory cell

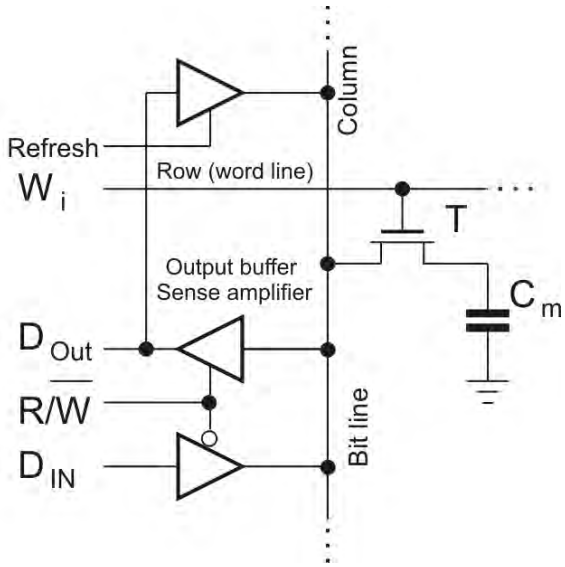


Reading a 0 from the memory cell

DRAM – Refresh Operation



Refreshing a stored 1



Refreshing a stored 0

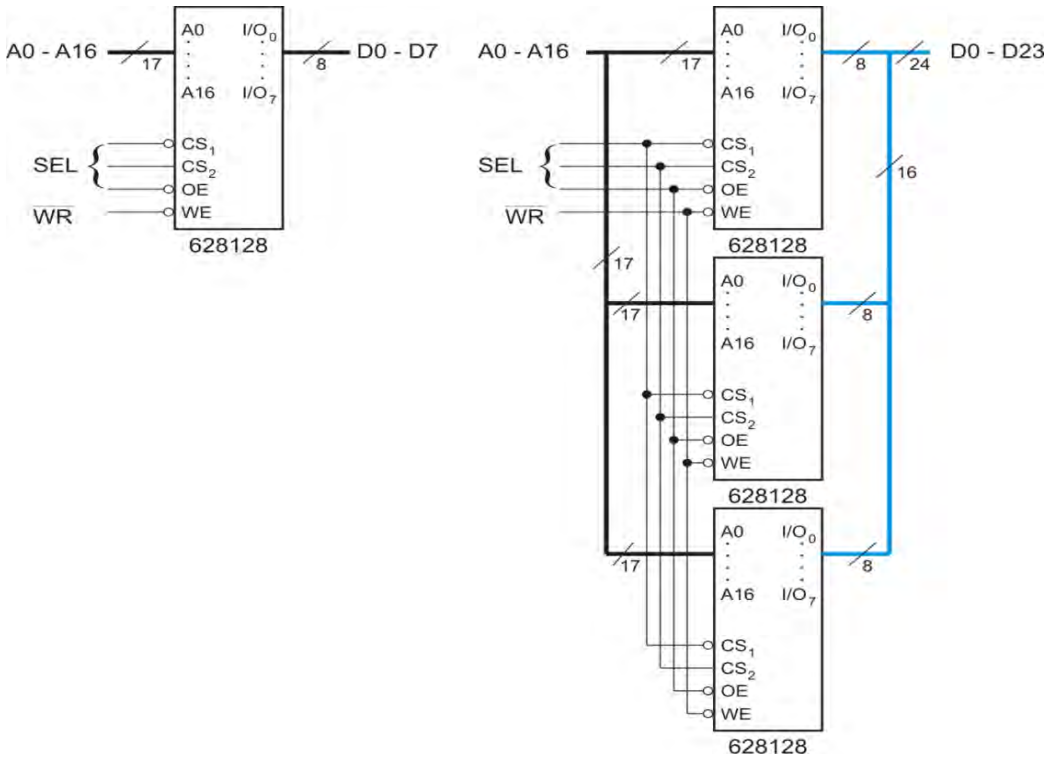
10. Memory extension techniques

Extending the Word Width

Word width extension 8 -> 24 bits

The initial memory

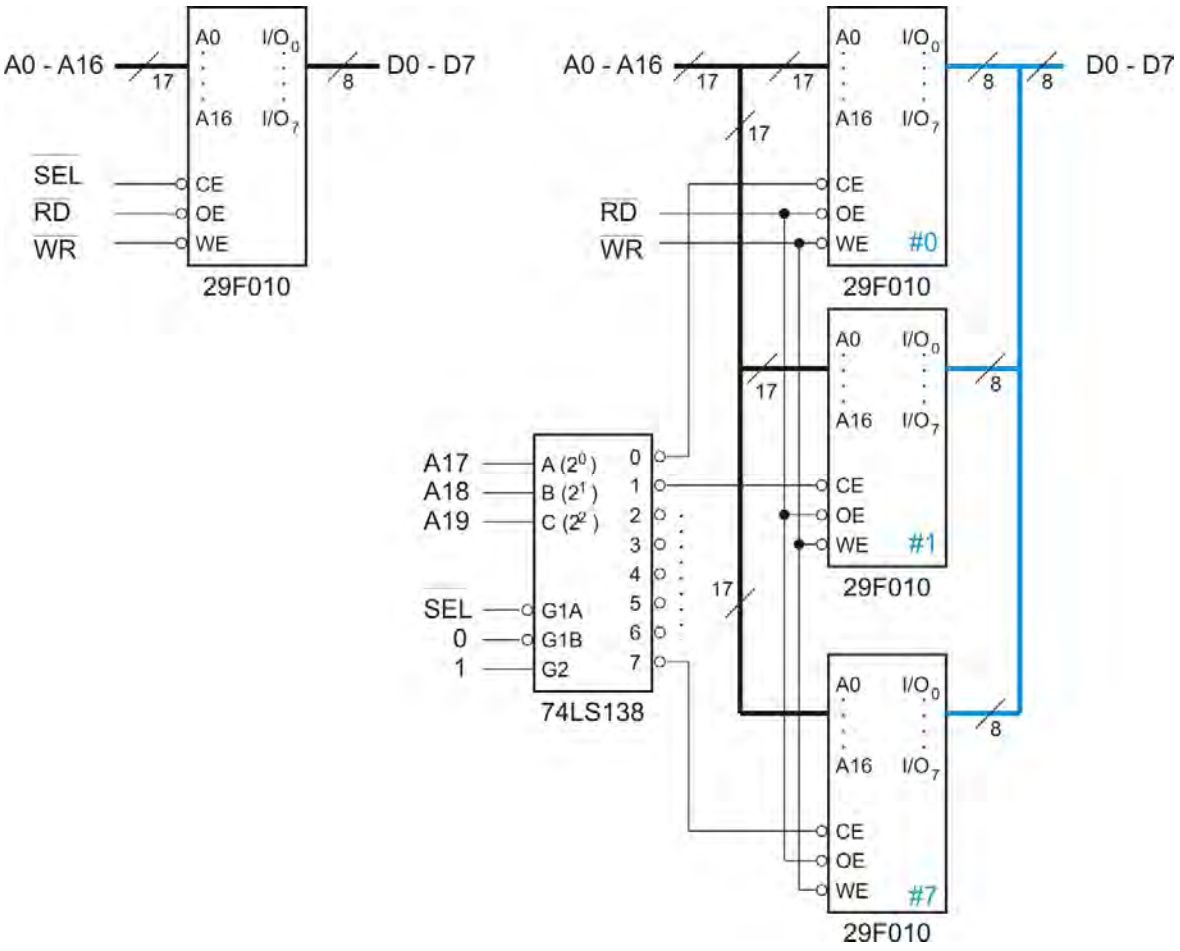
The extended memory



Extending the Number of Words

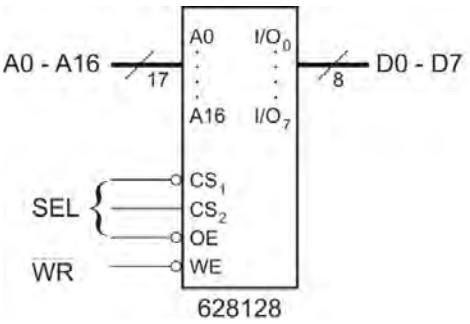
Extending the number of words (128 x 8 -> 1024 x 8 kbit)

The initial memory The extended memory

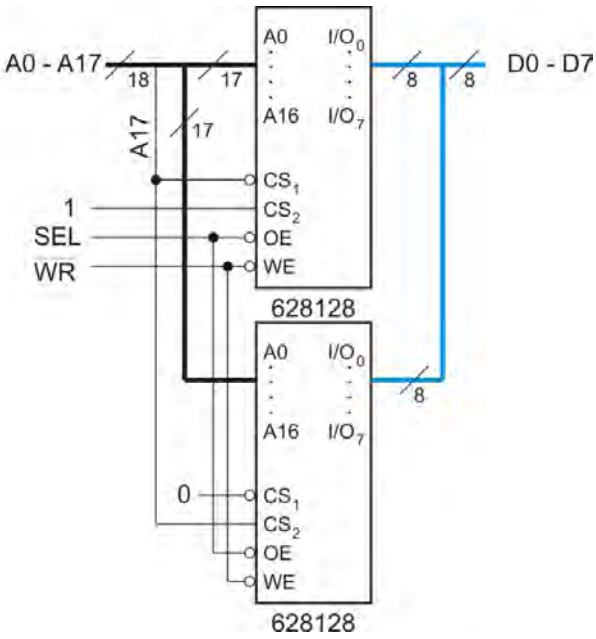

A0 - A16
17
A0
A16
I/O0
I/O7
8
D0 - D7
SEL
RD
WR
CE
OE
WE
29F010
A17
A18
A19
A (2^0)
B (2^1)
C (2^2)
G1A
G1B
G2
0
1
2
3
4
5
6
7
74LS138
#0
#1
#7

Doubling the capacity (128 to 256 kB)

The initial memory

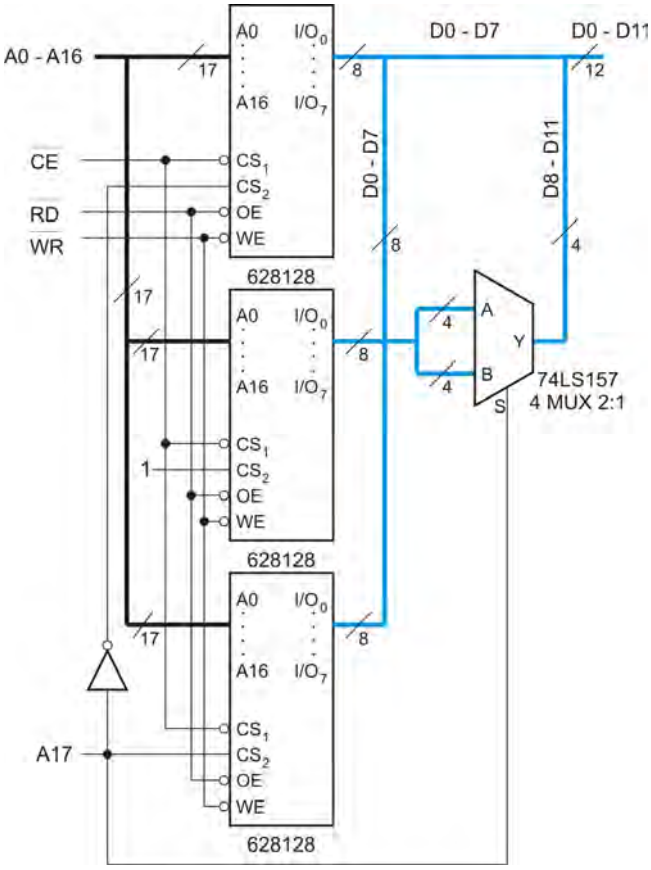


The extended memory



Mixed Extension

Mixed extension: 128 k x 8 bit -> 256 k x 12 bit



Analog Integrated Circuits

1. CC-CE, CC-CC and Darlington configurations – draw the schematics for these configurations and name the main parameters most often used to characterize these circuits. pg. 204, course #2

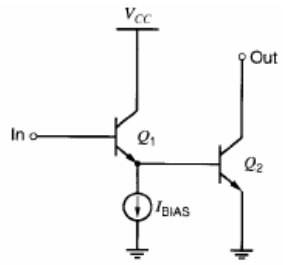


Fig. 1.

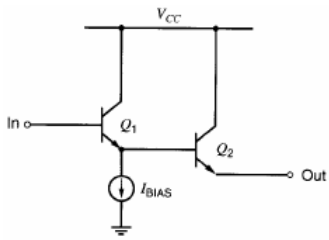


Fig. 2.

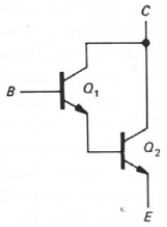


Fig. 3.

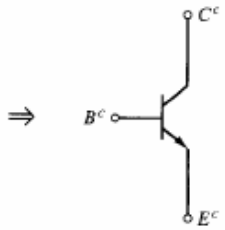


Fig.4.

(Abstract: These configuratios increase the input resistance and the current gain; the V_{BE} is twice the normal and the saturation voltage is at least V_{BE}.)

The common-collector - common-emitter (CC-CE), common-collector-common-collector (CC-CC), and Darlington configurations are all closely related. They incorporate an additional transistor to boost the current gain and input resistance of the basic bipolar transistor. The common-collector-common-emitter configuration is shown in Fig. 1. The biasing current source I_{BIAS} is present to establish the quiescent dc operating current in the emitter-follower transistor Ql**;** this current source may be absent in some cases or may be replaced by a resistor. The common-collector-common-collector configuration is illustrated in Fig. 2. In both of these configurations, the effect of transistor Q_l is to increase the current gain through the stage and to increase the input resistance.

The Darlington configuration, illustrated in Fig. 3, is a composite two-transistor device in which the collectors are tied together and the emitter of the first device drives the base of the second. A biasing element of some sort is used to control the emitter current of Ql**.** The result is a three-terminal composite transistor that can be used in place of a single transistor in common-emitter, common-base, and common-collector configurations. The term *Darlington* is often used to refer to both the CC-CE and CC-CC connections.

For the purpose of the low-frequency, small-signal analysis of circuits, the two transistors Q_l and Q_2 can be thought of as a single composite transistor, as illustrated in Fig. 4.

The composite transistor has much higher input resistance and current gain than a single transistor.

r_π^c is the resistance seen looking into the composite base BC with the composite emitter EC grounded (Fig 5):

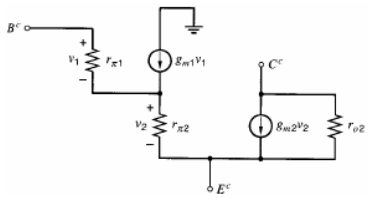


Fig. 5.

$$r_\pi^c = r_{\pi 1} + (\beta_0 + 1) r_{\pi 2}$$

For the special case in which the biasing current source I_{BIAS} is zero, the effective current gain β^c is the ratio:

$$\beta^c = \frac{i_c^c}{i_b^c} = \frac{i_{c2}}{i_{b1}}; = \frac{\beta_0 i_{b2}}{i_{b1}} = \frac{\beta_0 i_{e1}}{i_{b1}} = \frac{\beta_0(\beta_0+1) i_{b1}}{i_{b1}} = \beta_0(\beta_0+1)$$

The base-emitter drop is twice normal; the saturation voltage is at least one diode drop. The combination tends to act like a slow transistor; this is taken care of by including a resistor, R (few hundres Ohms – power transistor or a few thousend Ohms – small-signal Darlington).

2. *The bipolar cascode configuration – draw the circuit, compare its output resistance with that of the common emitter stage. pg. 207, course #2*

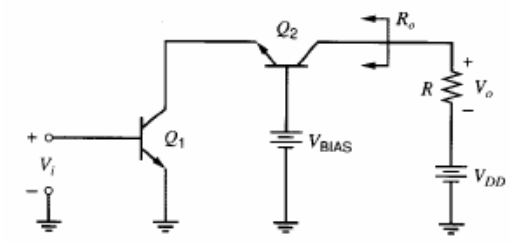


Fig. 6

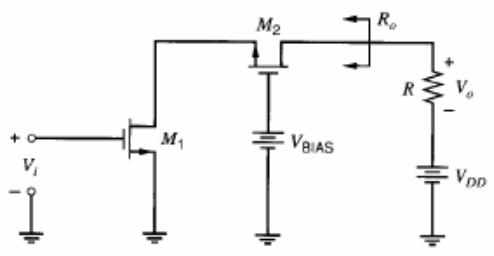


Fig. 7.

(Abstract: The cascode connection displays an output resistance that is larger by a factor of about β_0 than the CE stage alone.)

The cascode configuration is important mostly because it increases output resistance and reduces unwanted capacitive feedback in amplifiers, allowing operation at higher frequencies than would otherwise be possible. The high output resistance attainable is particularly useful in desensitizing bias references from variations in power-supply voltage and in achieving large amounts of voltage gain.

In bipolar form, the cascode is a common-emitter-common-base (CE-CB) amplifier, as shown in Fig. 6. The MOS version is shown in Fig. 7.The small-signal equivalent for the bipolar cascode circuit is shown in Fig. 8. The output resistance can be calculated by shorting the input v_i to ground and applying a test signal at the output. Then $v_1 = 0$ and the g_{mv1} generator is inactive (Fig. 9).

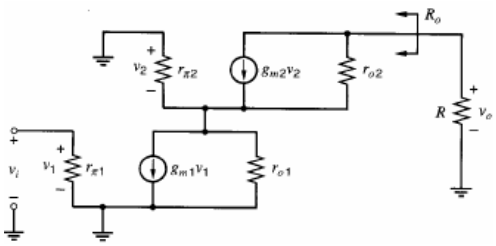


Fig. 8.

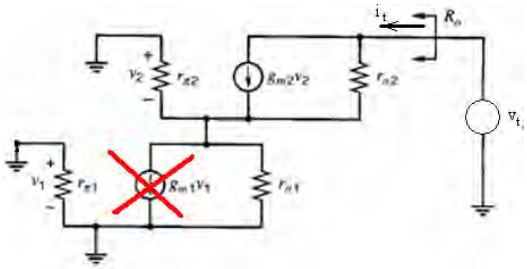


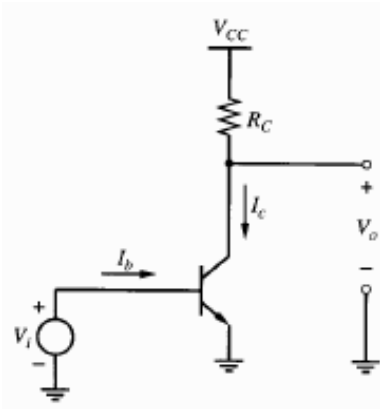
Fig. 9.

$$v_2 = -i_t\left(r_{\pi 2}\|r_{o1}\right) \qquad i_2 = i_t - g_{m2}v_2 = i_t\left[1 + g_{m2}\left(r_{\pi 2}\|r_{o1}\right)\right] \qquad v_t = -v_2 + i_2 \cdot r_{o2}$$

$$\Rightarrow R_o = \frac{v_t}{i_t} = r_{\pi 2}\|r_{o1} + r_{o2} + r_{o2}g_{m2}\cdot\left(r_{\pi 2}\|r_{o1}\right) \cong$$

$$\cong r_{o2}\left[1 + g_{m2}\cdot\left(r_{\pi 2}\|r_{o1}\right)\right] = r_{o2}\left[1 + g_{m2}\cdot\left(\frac{r_{\pi 2}r_{o1}}{r_{\pi 2} + r_{o1}}\right)\right] = r_{o2}\left(1 + \frac{g_{m2}r_{o1}}{1 + \frac{g_{m2}r_{o1}}{\beta_0}}\right)$$

If $g_{m2}r_{o1} >> \beta_0$ and $\beta_0 >> 1$ than $R_o \cong \beta_0 r_{o2}$



The cascode connection displays an output resistance that is larger by a factor of about β_0 than the CE stage alone (shown in Fig. 10) (we assumed that R_C is very large and can be neglected).

Fig. 10.

3. The dc transfer characteristic of an emitter-coupled pair - compare the schemes with and without emitter degeneration. We know the values for collector currents:

$$I_{c1} = \frac{\alpha_F I_{TAIL}}{1+\exp\left(-\frac{V_{id}}{V_T}\right)}; \qquad I_{c2} = \frac{\alpha_F I_{TAIL}}{1+\exp\left(\frac{V_{id}}{V_T}\right)}$$

pg. 215 – 217(abstract), course#2.

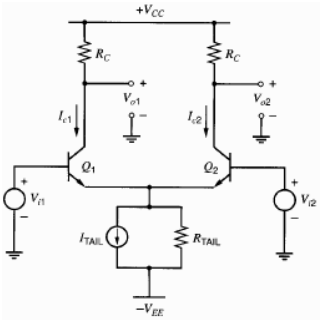


Fig. 11.

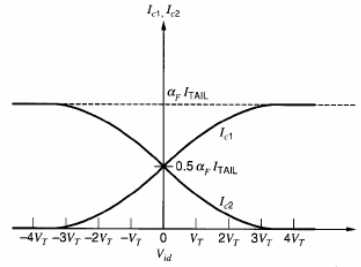


Fig. 12.

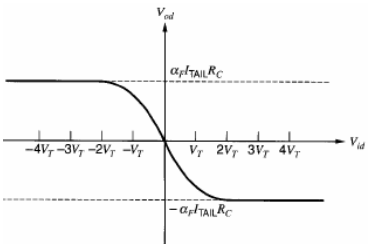


Fig. 13.

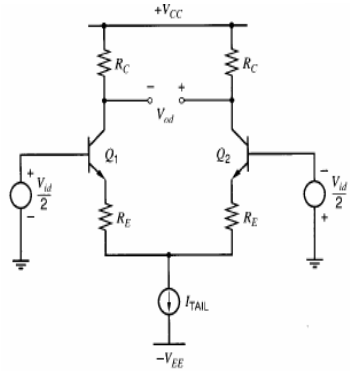


Fig. 14.

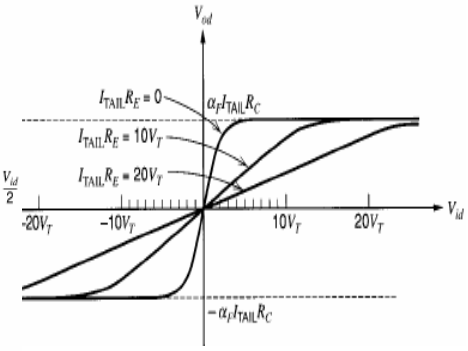


Fig. 15.

(Abstract: The circuit behaves in an linear fashion only when the magnitude of v_{id} is less than about V_T. The property „for v_{id}=0 we have v_{od}=0" allows direct coupling of cascaded stages. To increase the range of v_{id} emitter-degeneration resistors are included.)

The simplest form of an emitter-coupled pair is shown in Fig. 11. The large-signal behavior of the emitter-coupled pair is important in part because it illustrates the limited range of input voltages over which the circuit behaves almost linearly. These two currents are shown as a function of V_{id} in Fig. 12. When the magnitude of V_{id} is greater than about $3V_T$, the collector currents are almost independent of V_{id} because one of the transistors turns off and the other conducts all the current that flows. Furthermore, the circuit behaves in an approximately linear fashion only when the magnitude of V_{id} is less than about V_T . We can now compute the output voltages as:

$$V_{o1} = V_{cc} - I_{c1}R_C; \qquad V_{o2} = V_{cc} - I_{c2}R_C$$

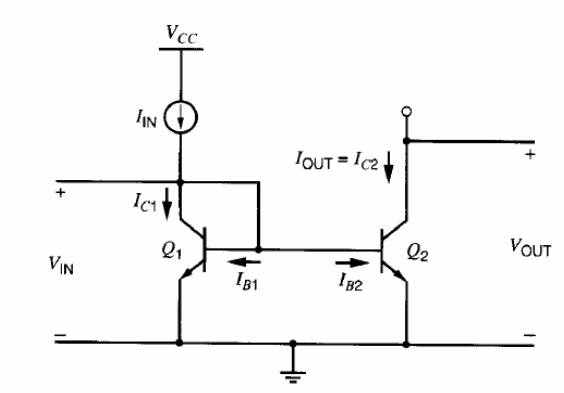
The output signal of interest is often the difference between V_{o1} and V_{o2}, which we define as V_{od}. Then:

$$V_{od} = V_{o1} - V_{o2} = \alpha_F I_{TAIL} R_C \tanh\left(\frac{-V_{id}}{2V_T}\right)$$

This function is plotted in Fig. 13. Here a significant advantage of differential amplifiers is apparent: when V_{id} is zero, V_{od} is zero if Q_1 and Q_2 are identical and if identical resistors are connected to the collectors of Q_1 and Q_2. This property allows direct coupling of cascaded stages without offsets.

To increase the range of V_{id} over which the emitter-coupled pair behaves approximately as a linear amplifier, emitter-degeneration resistors are frequently included, as shown in Fig.14. The effect of the resistors may be understood intuitively from the examples plotted in Fig. 15. For large values of emitter-degeneration resistors, the linear range of operation is extended by an amount approximately equal to I_{TAIL} R_E. Furthermore, since the voltage gain is the slope of the transfer characteristic, the voltage gain is reduced by approximately the same factor that the input range is increased.

4. *Simple current mirror - bipolar version. Draw the schematic and compare it with an ideal current mirror. pg. 256, course #4*



(Abstract : The output current for a simple current mirror must exactly mirror the input current but, in a real circuit, I_{OUT} is less then the input current, I_{IN}. Ideally**:** the output current is equal to the input current, independent of V_{OUT}, with $V_{IN} = 0$. A current mirror must provide a constant current at the output and an infinity output resistance.)

Fig. 16.

Ideally: the output current is equal to the input current multiplied by a desired current gain (if the gain is unity - **current mirror**); the current-mirrors gain is independent of input frequency; the output current is independent of the voltage between the output and common terminals; the voltage between the input and common terminals is ideally zero because this condition allows the entire supply voltage to appear across the input current source; more than one input and/or output terminals are sometimes used.

The simplest form of a current mirror consists of two transistors. Fig. 16 shows a bipolar version of this mirror. Transistor Q1 is diode connected, forcing its collector-base voltage to zero. In this mode, Q_1 operates in the forward-active region. Assume that Q_2 also operates in the forward-active region and that both transistors have infinite output resistance. Then I_{OUT} is controlled by $V_{BE2} = V_{BE1}$ (KVL).

$$V_{BE2} = V_T \ln\frac{I_{C2}}{I_{S2}} = V_{BE1} = V_T \ln\frac{I_{C1}}{I_{S1}}$$

$$\Rightarrow I_{C2} = \frac{I_{S2}}{I_{S1}} I_{C1} \quad \text{and if} \quad I_{S1} = I_{S2} \quad \text{shows that} \quad I_{C1} = I_{C2}$$

$$I_{IN} - I_{C1} - \frac{I_{C1}}{\beta_F} - \frac{I_{C2}}{\beta_F} = 0$$

$$I_{OUT} = I_{C2} = I_{C1} = \frac{I_{IN}}{1 + \frac{2}{\beta_F}}$$

$$\Rightarrow I_{C2} = \frac{I_{S2}}{I_{S1}} I_{C1} = \left(\frac{I_{S2}}{I_{S1}} I_{IN}\right)\left(\frac{1}{1 + \frac{1 + (I_{S2}/I_{S1})}{\beta_F}}\right)$$

In practice, the devices need not be identical.

At the input:

$$V_{IN} = V_{CE1} = V_{BE1} = V_{BE(on)}$$

Since $V_{BE(on)}$ is proportional to the natural logarithm of the collector current, V_{IN} changes little with changes in bias current.

The minimum output voltage required to keep Q_2 in the forward-active region is:

$$V_{OUT(min)} = V_{CE2(sat)}$$

5. Wilson current mirror – draw the schematic of the bipolar version, estimate the value of the output resistance and compare it with that of the cascode current mirror pg. 277, Course#6

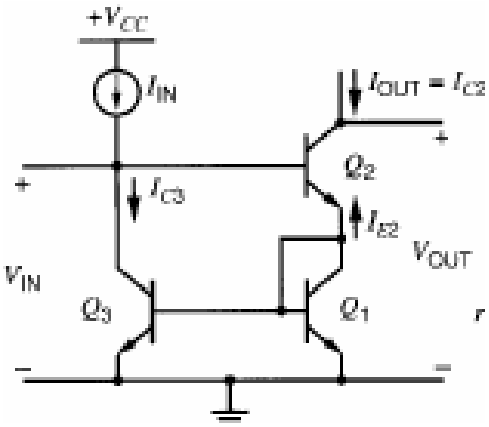


Fig. 17.

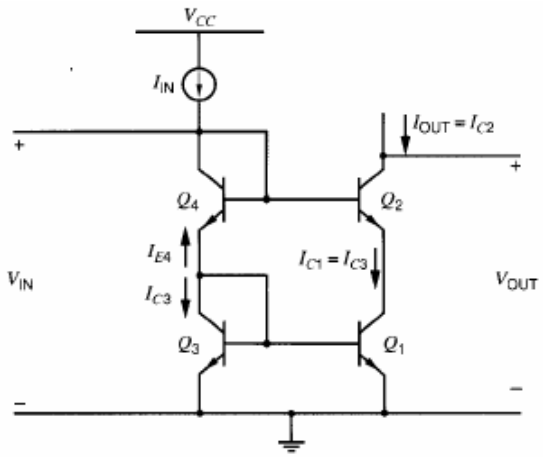


Fig. 18.

(Abstract: Both circuits, the Wilson current mirror and the cascode current mirror achieve a very high output resistance: $R_o \approx \frac{\beta_0 r_{o2}}{2}$)

The Wilson current mirror is shown in Fig. 17, the cascode current mirror is shown in Fig. 18. Both circuits, the Wilson current mirror and the cascode current mirror achieve a very high output resistance. A small - signal analysis shows that R_o, with some approximations, has the value:

$$R_o \approx \frac{\beta_0 r_{o2}}{2}$$

In the cascode current mirror, the small-signal current that flows in the base of Q2 is mirrored through Q3 to Ql so that the small-signal base and emitter currents leaving Q2 are approximately equal.

On the other hand, in the Wilson current mirror, the small-signal current that flows in the emitter of Q2 is mirrored through Q1 to Q3 and then flows in the base of Q2. Although the cause and effect relationship here is opposite of that in a cascode current mirror, the output resistance is unchanged because the small-signal base and emitter currents leaving Q2 are still forced to be equal. Therefore, the small-signal collector current of Q2 that flows because of changes in the output voltage still splits into two equal parts with half flowing in $r_{\pi 2}$.

6. Bipolar Widlar Current Source - draw the schematic, explain why it is not a current mirror. pg. 300, course#8

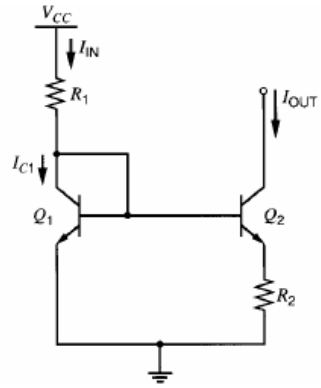


Fig. 19.

(Abstract: In the Widlar current source the transistors Q_1 and Q_2 operate with unequal base emitter voltages. This circuit is referred to as a current source rather than a current mirror because the output current, I_{OUT}, is much smaller than the input current, I_{IN}.)

In the Widlar current source of Fig. 19, the resistor R_2 is inserted in series with the emitter of Q_2, and transistors Q_1 and Q_2 operate with unequal base emitter voltages if $R_2 \neq 0$. This circuit is referred to as a current source rather than a current mirror because the output current is much less dependent on the input current and the power-supply voltage than in the simple current mirror.

Assume that Q_1 and Q_2 operate in the forward active region. KVL around the base-emitter loop gives:

$$V_{BE1} - V_{BE2} - \frac{\beta_F + 1}{\beta_F} I_{OUT} R_2 = 0 \qquad \Rightarrow V_T \ln \frac{I_{C1}}{I_{S1}} - V_T \ln \frac{I_{OUT}}{I_{S2}} - \frac{\beta_F + 1}{\beta_F} I_{OUT} R_2 = 0$$

$$\text{If} \quad \beta \to \infty \quad \text{and} \quad I_{s1} = I_{s1} \qquad \Rightarrow V_T \ln \frac{I_{IN}}{I_{OUT}} = I_{OUT} R_2$$

This transcendental equation can be solved by trial and error to find I_{OUT} if R_2 and I_{IN} are known, as in typical analysis problems. Because the logarithm function compresses changes in its argument, attention can be focused on the linear term, I_{OUT} R_2, simplifying convergence of the trial-and-error process. In design problems, however, the desired I_{IN} and I_{OUT} are usually known, and the equations provides the required value of R_2.

The Widlar source allows currents in the microamp range to be realized with moderate values of resistance. It is possible to write the final equation like this:

$$I_{IN} = I_{OUT} e^{\frac{I_{OUT} R_2}{V_T}}$$

It is obvious that I_{OUT} is much smaller than I_{IN}.

Exemple: I_{IN} = 1 mA, R2= 5 KΩ, I_{OUT} = 20 μA

7. Temperature-Insensitive Bias with band gap voltage reference: the motive, the idea, one of the practical implementations. Pg. 317, course #9

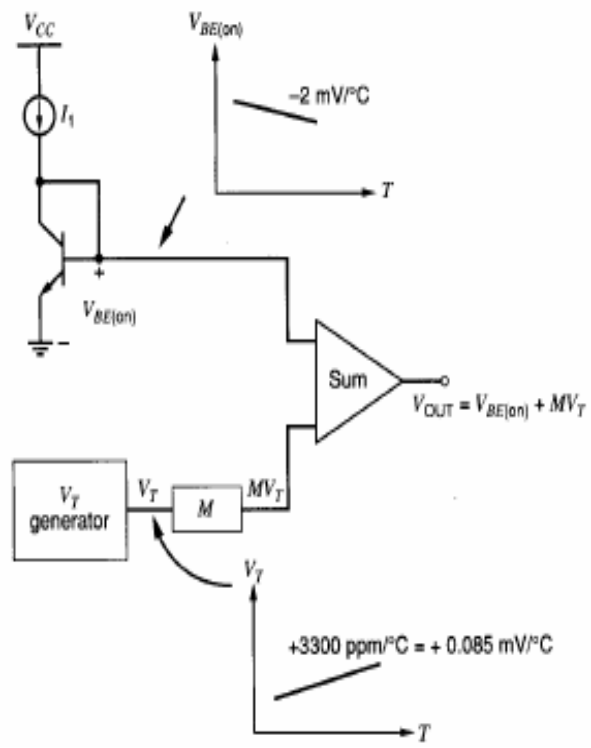


Fig. 20.

(Abstract: We need low-temperature-coefficient reference voltages. The idea is shown in Fig. 20. – 2mV/°C temperature-coefficient of V_{BE} to be compensated with a component with +2mV/°C coefficient temperature.)

In practice, requirements often arise for low-temperature-coefficient voltage bias or reference voltages. The voltage reference for a voltage regulator is a good example.

Since $V_{BE(on)}$ and V_T have opposite T_{CF}, the possibility exists for referencing the output current to a composite voltage that is a weighted sum of $V_{BE(on)}$ and V_T. By proper weighting, zero temperature coefficient should be attainable. So we can obtain low-temperature-coefficient voltage bias or reference voltages.

$$V_{OUT} = V_{BE(on)} + MV_T$$

The idea is shown in Fig. 20. – 2mV/°C temperature-coefficient of V_{BE} to be compensated with a component with +2mV/°C coefficient temperature. One possibility is to use V_T which T_{CF} is about +0,085 mV/°C.

A bandgap voltage reference is a voltage reference circuit widely used in integrated circuits usually with an output voltage around 1.25 V, close to the theoretical band gap of silicon at 0°K. A practical implementation is shown in Fig. 21.

$$V_{RC1} = V_{RC2} \Rightarrow I_{C1} = I_{C2}$$

$$V_{R1} = I_{C1}R_1 = V_{BE2} - V_{BE1} =$$

$$= V_T \ln\frac{I_{C2}}{I_S} - V_T \ln\frac{I_{C1}}{I_S} = V_T \ln\frac{I_{C2}}{I_{C1}} = V_T \ln n$$

$$V_{R2} = R_2(I_{C1} + I_{C2}) = R_2\left(\frac{V_T \ln n}{R_1} + n\frac{V_T \ln n}{R_1}\right) =$$

$$= \frac{R_2}{R_1}(n+1)V_T \ln n = N \cdot V_T$$

$$\frac{dV_{R2}}{dT} = N\frac{dV_T}{dT} = N\frac{k}{q} = N\frac{kT}{qT} = N\frac{V_T}{T} = +2\frac{mV}{^\circ C}$$

$$\Rightarrow N = 2\cdot 10^{-3}\,\frac{300}{26\cdot 10^{-3}} \cong 23$$

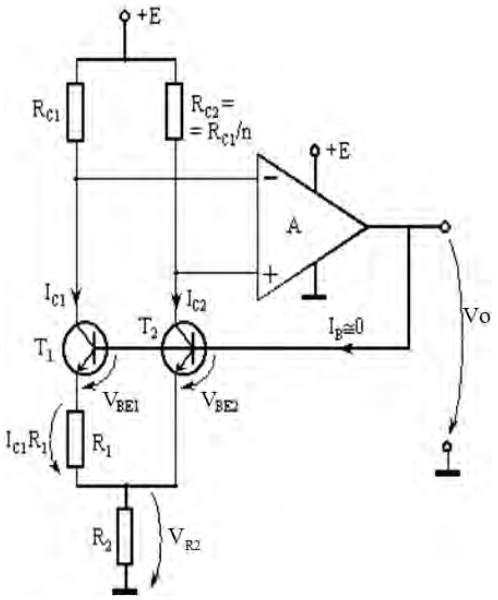


Fig. 21.

8. *Inverting and noninverting amplifier built with an ideal op amp - draw the schematics and find the gains, define the characteristics of an ideal op amp. pg. 406, 408, course #9*

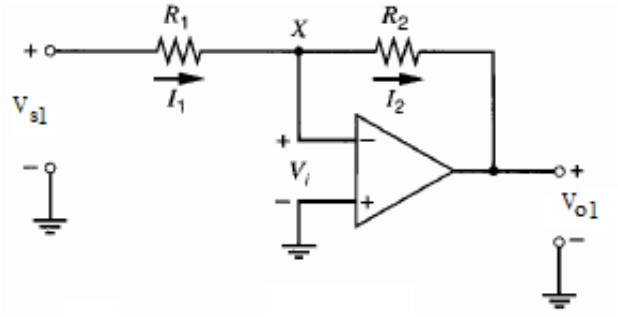


Fig. 22.

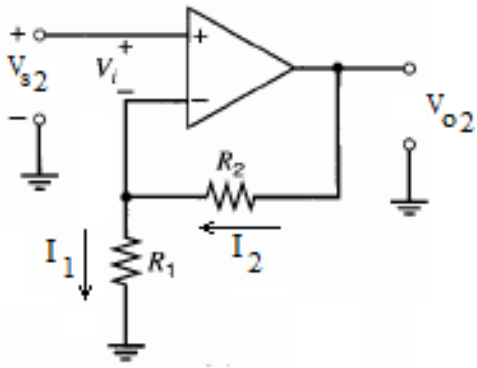


Fig. 23.

(Abstract: The golden rules: 1.The output attempts to do whatever is necessary to make the voltage difference between the inputs zero (in Fig. 22 and Fig. 23, $V_i = 0$). 2.The inputs draw no current)

An ideal op amp with a single-ended output has a differential input, infinite voltage open-loop gain, infinite input resistance, and zero output resistance. While actual op amps do not have these ideal characteristics, their performance is usually sufficiently good that the circuit behavior closely approximates that of an ideal op amp in most applications. These characteristics lead to the golden rules for op-amps. They allow us to logically deduce the operation of any op-amp circuit.

Fig. 22 shows an inverting amplifier build with an op amp. Considering we have an ideal op amp. First, because no current enters in the ”-” input, at the nod X we can write:

$$I_1 = I_2 \qquad (1)$$

Second, $V_i = 0$ and at the inverting input we have a ” virtual ground”. Then the voltage V_{s1} is across R_1 and Vo1 is across R_2. In the first equation we can replace I_1 and I_2 with the values:

$$I_1 = \frac{V_{s1}}{R_1} \qquad I_2 = \frac{-V_{o1}}{R_2}$$

Equation (1) becames:

$$\frac{V_{s1}}{R_1} = -\frac{V_{o1}}{R_2} \Leftrightarrow V_{o1} = -V_{s1}\frac{R_2}{R_1}$$

This is the relationship between the output voltage and the input voltage for an inverting amplifier build with an op amp. A similar calculation can be done for the noninverting amplifier build with an ideal op amp (Fig. 23). The same, for Fig. 23:

$$I_1 = I_2 \qquad (2)$$

But we don’t have a virtual ground anymore: at the noninverting input is V_{s2}. In this case we can write:

$$I_1 = \frac{V_{s2}}{R_1} \qquad I_2 = \frac{V_{o2} - V_{s2}}{R_2}$$

Using this values in (2) we get the relationship between the output voltage and the input voltage for a noninverting amplifier build with an op amp:

$$\frac{V_{s2}}{R_1} = \frac{V_{o2} - V_{s2}}{R_2} \Leftrightarrow V_{o2} = \left(1 + \frac{R_2}{R_1}\right)V_{s2}$$

9. *Integrator, differentiator build with op amp - draw the schematics, find the relationships between input and output voltages. pg. 410, Course #10*

The integrator (Fig. 24) and the differentiator circuits (shown in Fig. 25) are examples of using op amps with reactive elements in the feedback network to realize a desired frequency response or time-domain response.

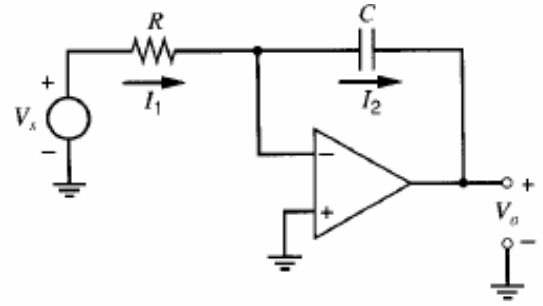


Fig. 24.

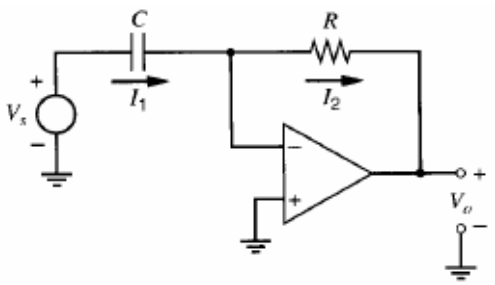


Fig. 25.

(Abstract: In the case of the integrator the output voltage is proportional to the integral of the input voltage with respect to time. In the case of the differentiator the output voltage is proportional to the time rate of change of the input voltage.)

In the case of the integrator (Fig. 24), the resistor R is used to develop a current I_1 that is proportional to the input voltage, V_s. This current flows into the capacitor C, whose voltage is proportional to the integral of the current I_2 with respect to time. Since the output voltage is equal to the negative of the capacitor voltage, the output is proportional to the integral of the input voltage with respect to time. In terms of equations:

$$I_1 = \frac{V_s}{R} = I_2 \qquad V_o = -\frac{1}{C}\int_0^t I_2 d\tau + V_o(0) \quad \Rightarrow V_o(t) = -\frac{1}{RC}\int_0^t V_s(\tau)d\tau + V_o(0)$$

In the case of the differentiator (Fig. 25), the capacitor C is connected between V_s and the inverting op-amp input. The current through the capacitor is proportional to the time derivative of the voltage across it (V_c), which is equal to the input voltage ($V_c = V_s$). This current flows through the feedback resistor R, producing a voltage at the output proportional to the capacitor current, which is proportional to the time rate of change of the input voltage. In terms of equations:

$$I_1 = C\frac{dV_s}{dt} = I_2 \qquad V_o = -RI_2 = -RC\frac{dV_s}{dt}$$

10. Improved precision half-wave rectifier - draw the schematic, the equivalent ones, the diadrames and explain the operation. pg.705, Course #10

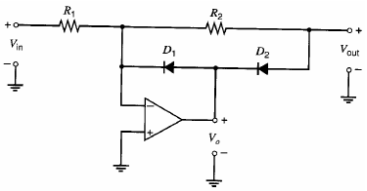


Fig. 26.

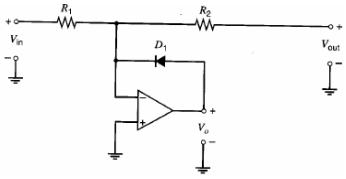


Fig. 27.

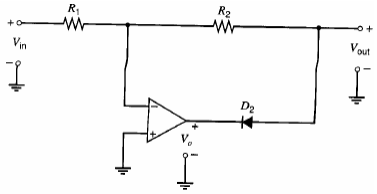


Fig. 28.

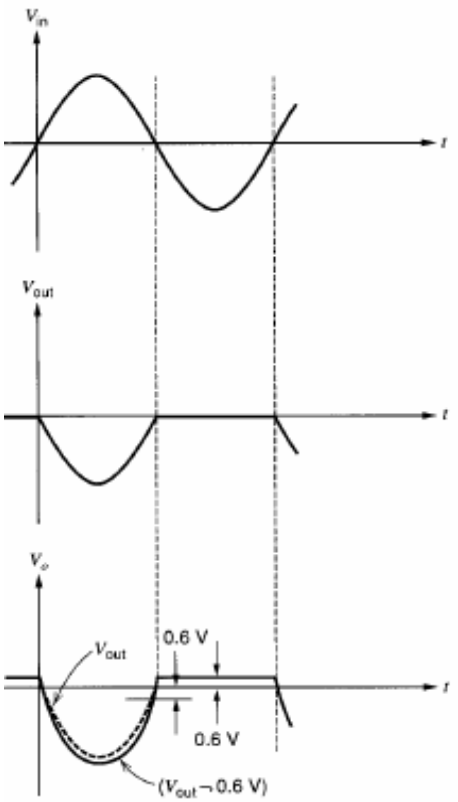


Fig. 29

(Abstract: The schematic for an improved precision half-wave rectifier is shown in Fig. 26. Fig. 27 shows the equivalent circuit for $V_i<0$ and Fig. 28 shows the equivalent circuit for $V_i>0$. Fig. 29 shows the waveforms within the improved precision rectifier for a sinusoidal input, V_{in}; the output of the circuit is V_{out} and V_o is the op amp's output.)

For input voltages less than zero, the equivalent circuit is shown in Fig. 27. Diode D_1 is forward biased and the op amp is in the active region. The inverting input of the op amp is clamped at ground by the feedback through D_1, and, since no current flows in R_2, the output voltage is also at ground. When the input voltage is made positive, no current can flow in the reverse direction through D_1 so the output voltage of the op amp V_o is driven in the negative direction. This reverse biases D_1 and forward biases D_2. The resulting equivalent circuit is shown in Fig. 28 and is simply an inverting amplifier with a forward-biased diode in series with the output lead of the op amp. Because of the large gain of the op amp, this diode has no effect on its behavior as long as it is forward biased, and so the circuit behaves as an inverting amplifier giving an output voltage of:

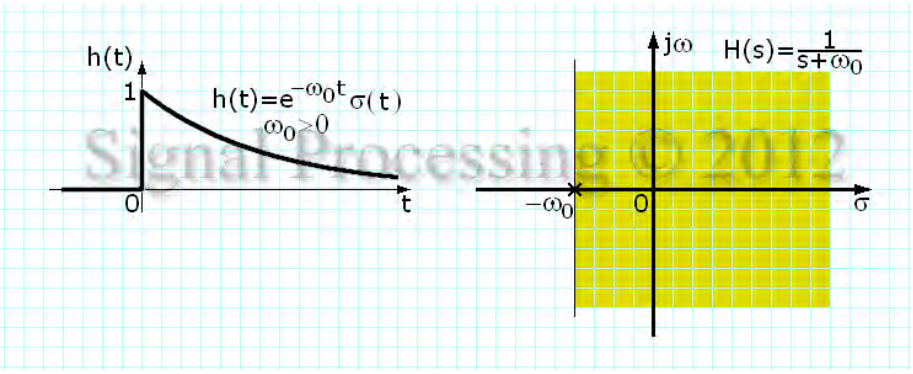
$$V_{out} = -\frac{R_2}{R_1} V_{in}$$

As shown in Fig. 29, the output voltage of the operational amplifier need only change in value by approximately two diode drops when the input signal changes from positive to negative.

Signal Processing

1. *Where are the poles of a stable and causal analog system? Give an example.*

The poles of a stable and causal system are located in the left half plane LHP while its zeros can be located anywhere in the complex plane. Example: $h(t)=\exp(-\omega_0 t)\sigma(t), \omega_0>0$. The transfer function is $H(\omega)=\frac{1}{s+\omega_0}$ with one pole, $s_p=-\omega_0$.



2. *Define minimum phase analog systems. Give an example.*

Systems having poles and zeros placed in the left half plane are named minimum phase systems. Consider the system with the impulse response

$h(t)=e^{-t}\sigma(t)\leftrightarrow H_u(s)=\frac{1}{s+1}$. It has one pole in the LHP and no zeros; hence it is a minimum phase system:

$H(\omega)=\frac{1}{1+j\omega}$, with $|H(\omega)|=1/\sqrt{1+\omega^2}, \Phi(\omega)=-arctg\omega$.

as opposed to another system with the frequency response:

$$H_{\omega_0}(\omega)=\frac{1}{1+j\omega}\frac{1-j\frac{\omega}{\omega_0}}{1+j\frac{\omega}{\omega_0}}\longleftrightarrow h_{\omega_0}(t)=\frac{1}{\omega_0-1}\left[(\omega_0+1)e^{-t}-2\omega_0 e^{-\omega_0 t}\right]\sigma(t)$$

with $\Phi_{\omega_0}(\omega)=-arctg\omega-2arctg\frac{\omega}{\omega_0}=\Phi(\omega)-2arctg\frac{\omega}{\omega_0}$.

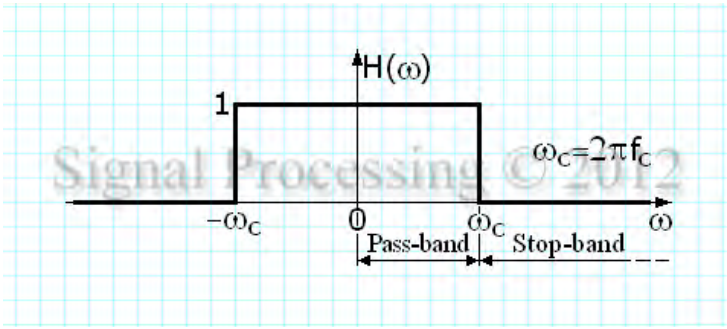
Both systems have the same amplitude-frequency characteristic but the second system introduces extra phase versus the first system.

3. *Ideal low pass filter. Frequency response and impulse response.*

The ideal low pass filter has the frequency response:

$$H(\omega) = p_{\omega_c}(\omega) \leftrightarrow h(t) = \frac{\sin \omega_c t}{\pi t}$$

It does not fulfill Paley-Wiener theorem.



4. *Enunciate WKS sampling theorem.*

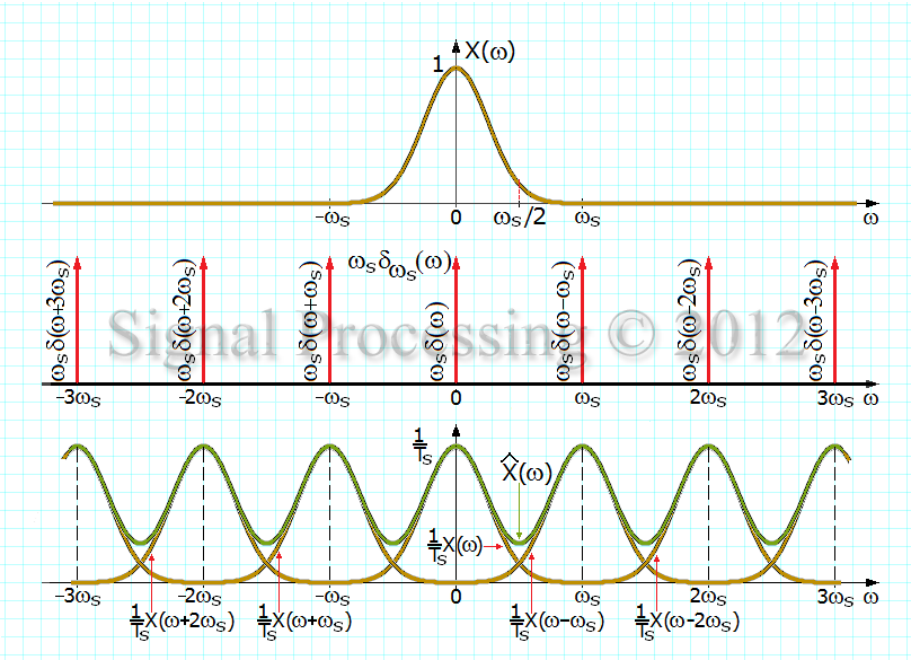
If the finite energy signal $x(t)$ is band limited at ω_M , ($X(\omega)=0$ for $|\omega| > \omega_M$), it is uniquely determined by its samples $\{x(nT_s) | n \in \square\}$ if the sampling frequency is higher or equal than twice the maximum frequency of the signal:

$$\omega_s \geq 2\omega_M$$

5. *Spectrum of ideal sampled signal (Relation + Graphical representation).*

$$\hat{x}(t) = \sum_{k=-\infty}^{\infty} x(kT_s)\delta(t - kT_s) \leftrightarrow \hat{X}(\omega) = \frac{1}{T_S} \sum_{k=-\infty}^{\infty} X\left(\omega - k\frac{2\pi}{T_S}\right)$$

The spectrum of an ideal sampled signal is the periodic repetition of the spectrum of the original signal. The period is inverse proportional with the sampling step T_S.

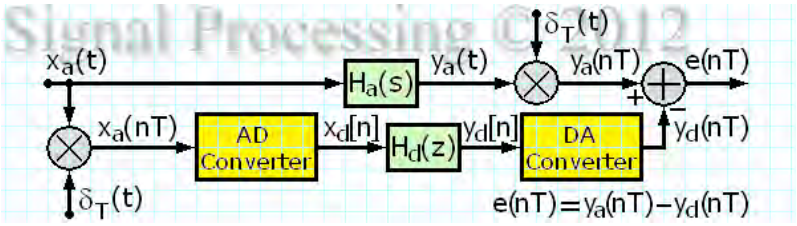


Spectrum of original signal

Spectrum of periodic Dirac distribution

Spectrum of ideal sampled signal

6. *Approximation of continuous-time systems with discrete-time systems using impulse invariance method.*



The system (not necessarily band-limited) is identified using input signal of the analog system the Dirac impulse. The impulse response of the analog system is sampled to produce the impulse response of the digital system.

for $x_a(t)=\delta(t)\Rightarrow y_a(t)=h_a(t)$; $x_d[n]=\frac{1}{T}\delta[n]$; $y_a(nT)=h_a(nT)$.

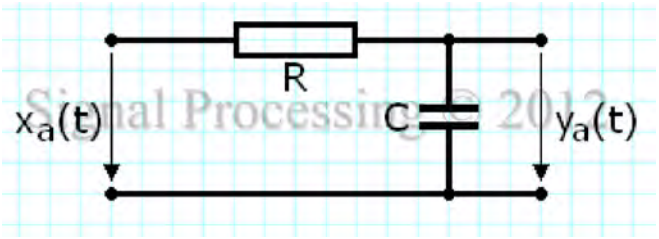
$$y_d[n]=\frac{1}{T}\delta[n]*h_d[n]=\frac{1}{T}h_d[n]$$

The error is smallest for: $h_d[n]=Th_a(nT)$

The frequency response of the digital system is the same with the frequency response of the analog system of limited band for frequency less than half of the sampling frequency

$$H_a(\omega) = H_d(\Omega)\big|_{\Omega=\omega T};\quad |\omega| \le \frac{\pi}{T} \text{ and } \omega_M \le \frac{\pi}{T}$$

7. *Approximation of RC circuit using bilinear transform method.*



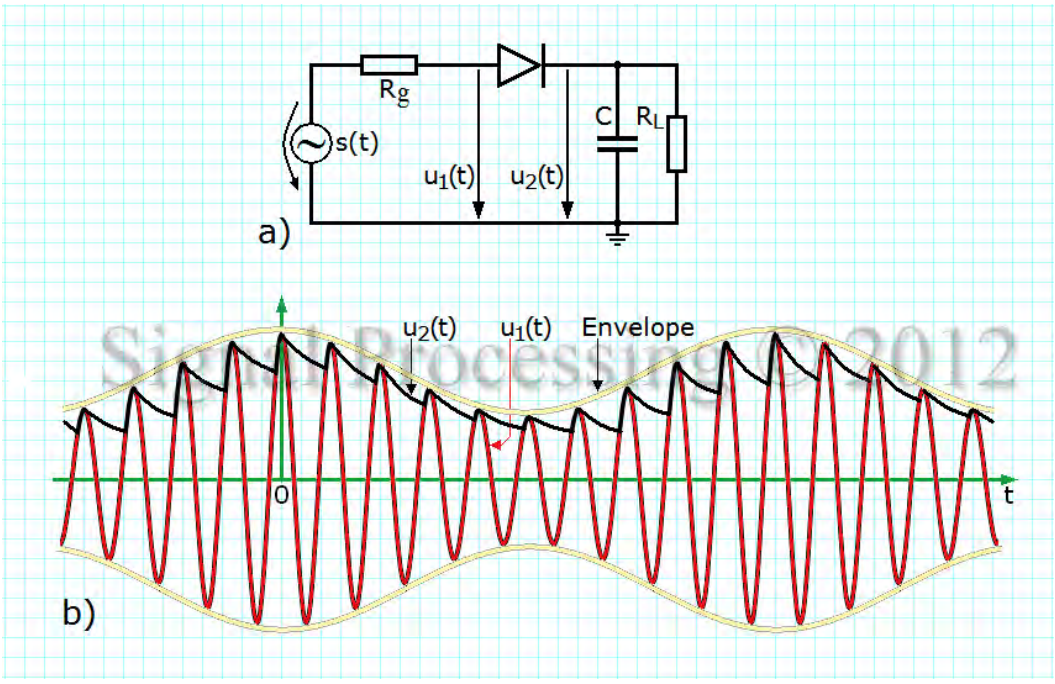
time constant: $\tau = RC = \frac{1}{\omega_0};\quad H_a(s) = \frac{1}{1+s\tau}$

$$s = \frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}};\qquad H_d(z) = H_a(s)\Big|_{s=\frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}}}$$

$$\Rightarrow H_d(z) = \frac{\frac{T}{T+\tau}}{1-\frac{\tau}{T+\tau}z^{-1}}$$

8. *Demodulator (envelope detector) for AM signals.*

AM demodulation can be realized using an envelope detector. For $R_g << R_s$, the voltage from the capacitor $u_2(t)$ follows the voltage $u_1(t)$ if the latter is high enough and the diode conducts (on the positive half-cycle of the input signal). When the diode becomes reverse biased, the capacitor discharges through the resistor R_L. The modulating wave is reconstructed using low pass filtering and removal of the DC component for $u_2(t)$.



9. *Narrow Band Frequency Modulation.*

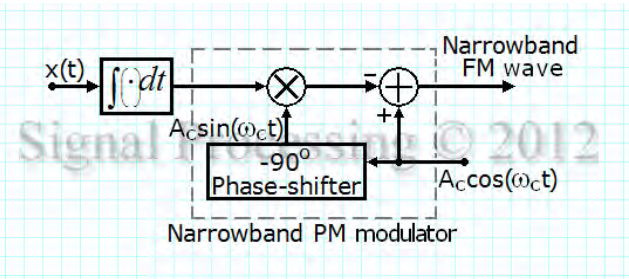
FM signal's expression is: $s(t) = A_c \cos\theta_i(t) = A_c \cos\left[\omega_c t + \beta \sin \omega_m t\right]$, where the modulating wave to be transmitted is $x(t) = A_m \cos \omega_m t$. Depending on the value of the modulation index $\beta = \Delta\omega / \omega_m$, we have narrow band FM ($\beta << 1$ radian) or wide band FM ($\beta >> 1$ radian). For narrow band FM, the modulated wave is:

$$s(t) = A_c \cos\omega_c t \cos(\beta \sin \omega_m t) - A_c \sin\omega_c t \sin(\beta \sin \omega_m t).$$

If $\beta < \dfrac{\pi}{36}$ rad $\Rightarrow \cos(\beta \sin \omega_m t) \cong 1$ and $\sin(\beta \sin \omega_m t) \cong \beta \sin \omega_m t$

$$\Rightarrow s(t) = A_c \cos\omega_c t - \beta A_c \sin\omega_c t \sin\omega_m t.$$

A possible implementation scheme is shown below.

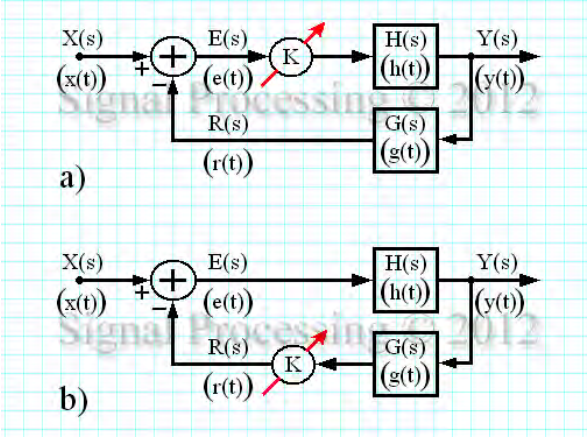


There are two disadvantages:

1-the envelope is affected by residual amplitude modulation so it varies in time,

2-for a harmonic modulating wave, the angle $\theta_i(t)$ contains other harmonics (order 3 and superior) of the modulating frequency, ω_m, so it is distorted.

10. Nyquist stability criterion for continuous-time systems when the open loop system is stable (schema + enunciation).



a) $$\frac{Y(s)}{X(s)} = \frac{KH(s)}{1+KH(s)G(s)}$$

b) $$\frac{Y(s)}{X(s)} = \frac{H(s)}{1+KH(s)G(s)}$$

-If the open loop system is stable then $H(s)G(s)$ doesn't have poles in the right half plane or on the imaginary axis. So, the open loop Nyquist's hodograph G(jω)H(jω) **doesn't make complete rotations** around the point (-1/K,0)

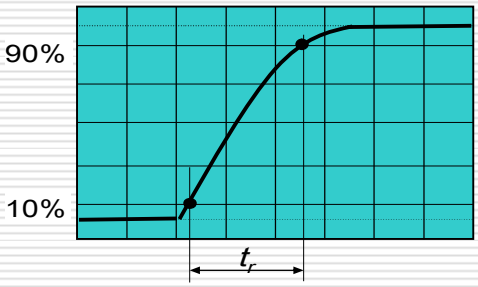
-Since $h(t)$ and $g(t)$ are real functions, Nyquist's hodograph for $\omega \in (-\infty,0)$ is obtained by **symmetry** with respect to the real axis of the complex plane $H(s)G(s)$ from the Nyquist's hodograph for $\omega \in (0,\infty)$

1. *General purpose analog oscilloscopes. Relationship between bandwidth and rise time of an oscilloscope. Determine the rise time of a 20 MHz oscilloscope.*

https://intranet.etc.upt.ro/~E_INSTR/PowerPoint%20presentations%202010%202011/1%20Oscilloscopes%202010%202011.ppt , slide #18

General purpose analog oscilloscopes

Oscilloscope's rise time



Relationship between bandwidth and rise time

$$t_r\,(\text{ns}) = \frac{350}{B\,(\text{MHz})}$$

Exercise. Determine the rise time of a 50 MHz oscilloscope.

(Answer: 7 ns)

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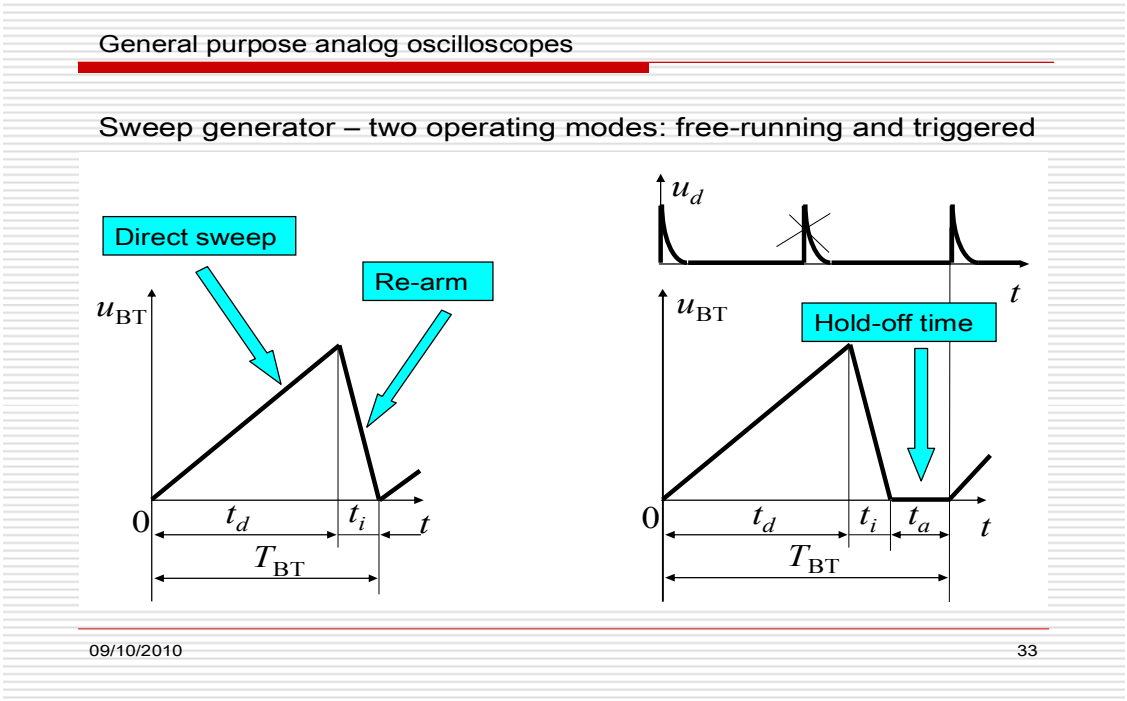
Answer: The rise time of a 20 MHz oscilloscope is 17 ns.

2. *General purpose analog oscilloscopes. Describe the free-running and the triggered modes of operation of the time base.*

https://intranet.etc.upt.ro/~E_INSTR/PowerPoint%20presentations%202010%202011/1%20Oscilloscopes%202010%202011.ppt, slides #33-38



With triggered sweeps, the scope will blank the beam and start to reset the sweep circuit (re-arm) each time the beam reaches the extreme right side of the screen. For a period of time, called *hold-off*, the sweep circuit resets completely and ignores triggers. Once hold-off expires, the next trigger starts a sweep. The trigger event is usually the input waveform reaching some user-specified threshold voltage (trigger level) in the specified direction (going positive or going negative - trigger polarity). Triggering circuit ensures a stable image on the screen.

Triggering condition $T_{BT} = kT_Y$

The sweep generator's period should be a multiple of the signal period. Timing diagrams (triggered sweep):