UNIVERSITATEA “POLITEHNICA” DIN TIMIŞOARA

Faculty of Electronics and Telecommunications

Studies in English

BACHELOR FINAL EXAM

Academic Year 2012-2013

UNIVERSITATEA “POLITEHNICA” DIN TIMIŞOARA
Faculty of Electronics and Telecommunications
Studies in English

BACHELOR FINAL EXAM

Academic Year 2012-2013

Table of contents

Core Courses

Mathematics……...1

Physics……..10

Measuring units……14

Electronic circuits…….16

Digital integrated circuits…….32

Analog integrated circuits……53

Signal processing……..66

Electronic instrumentation……...72

Fifth thematic area (applications)…… ……...87

Major Courses

Radio communications……....98

Power electronics……...104

Embedded Systems……..115

Electronic equipment testing……..124

Integrated digital networks…….131

Data communications……145

Audio and video systems……157

Mathematics

1. *Present Taylor's formula for functions of one variable and how can be used in approximating functions by polynomials.*

Answer:

Let $f : I \subset \mathbf{R} \to \mathbf{R}$, and $x_0 \in I$, where $f \in C^{n+1}(I)$. Then $f(x) = T_n(x) + R_n(x)$ (*Taylor's formula*),

where T_n is the Taylor's polynomial of n[th] order, and R_n is the reminder:

$$T_n(x) = f(x_0) + \frac{x - x_0}{1!} f'(x_0) + \ldots + \frac{(x - x_0)^n}{n!} f^{(n)}(x_0),$$

$$R_n(x) = \frac{(x - x_0)^{n+1}}{(n+1)!} f^{(n+1)}(x_0 + \theta(x - x_0)),\ 0 < \theta < 1.$$

It follows the approximation formula for $f(x)$ in a neighborhood V of x_0:

$$f(x) \cong T_n(x),$$

with the error $\varepsilon_n = \sup_{x \in V} |R_n(x)|$.

2. *Define the notions of eigenvalue (or proper value) and eigenvector (or proper vector) on a linear operator.*

***Answer*:**

We consider the vector space V defined over the field **K** and the linear operator $f : V \to V$. A vector v V (different from the null vector of V) is called an eigenvector (or proper vector) of the operator f if there exists a scalar λ from **K** such that $f(v) = \lambda v$. The scalar λ is called an eigenvalue (or proper value) of f.

3. Specify how the extremes of a function of class C^2 of two variables can be found.

Answer:

The extremes of the function $u = u(x, y)$ are among the *stationary points*, namely the solutions of the system $\begin{cases} \dfrac{\partial u}{\partial x} = 0 \\ \dfrac{\partial u}{\partial y} = 0 \end{cases}$.

A stationary point is a point of *minimum* if in this point

$$\frac{\partial^2 u}{\partial x^2} \cdot \frac{\partial^2 u}{\partial y^2} - \left(\frac{\partial^2 u}{\partial x \partial y} \right)^2 > 0 \text{ and } \frac{\partial^2 u}{\partial x^2} > 0,$$

and is a point of *maximum* if in this point

$$\frac{\partial^2 u}{\partial x^2} \cdot \frac{\partial^2 u}{\partial y^2} - \left(\frac{\partial^2 u}{\partial x \partial y} \right)^2 > 0 \text{ and } \frac{\partial^2 u}{\partial x^2} < 0.$$

4. Define the following notions: arithmetical mean, weighted arithmetical mean and geometrical mean.

***Answer*:**

Let $\{x_1, x_2, \ldots, x_n\}$ be a non-empty set of records (real numbers) with non-negative wedges $\{p_1, p_2, \ldots, p_n\}$.

Weighted mean: $M_p = \dfrac{p_1 x_1 + p_2 x_2 + \cdots + p_n x_n}{p_1 + p_2 + \cdots p_n}$ (the elements with a greater weight have more contribution to the mean). We can simplify the above formula taking normalized weights $\sum_{i=1}^{n} p_i = 1$. In this case we have $M_p = \sum_{i=1}^{n} p_i x_i$

Arithmetical mean : M_a it is a particular case of the weight mean M_p when all weights are equals $p_n = \frac{1}{n}$.

We have $M_a = \frac{1}{n}\sum_{i=1}^{n} x_i = \frac{x_1 + x_2 + \cdots + x_n}{n}$ (M_a indicates the central trend of a set numbers).

Geometrical mean : $M_g = \sqrt[n]{x_1, x_2, \cdots x_n}$ if $x_i > 0$, $i = \overline{1,n}$. The geometrical mean has the following geometric explanation: the geometrical mean $M_g = \sqrt{a\,b}$ of two numbers a, $b \in \mathbf{R}_+$ represents the length of a square with the same area as a rectangle with lengths a and b.

5. Define the notion of the conditional probability, write and explain the Bayes's formula.

***Answer*:**

Let $\{E, K, P\}$ a probability space and $A, B \in K$ two events with $P(A) \neq 0$. We call the probability of the event B conditioned by the event A, the expression:

$$P_A(B) = P(B/A) = \frac{P(A \cap B)}{P(A)}$$

Let $S = \{B_1, B_2 \ldots B_n\}$ an events complete system. Therefore, $E = \bigcup_{i=1}^{n} B_i, B_i \in K, B_i \bigcap B_j = \phi, i \neq j$. We say that the system S is a partition of the sure event E, and the events B_i are called outcomes.

Bayes's formula:

$$P_A(B_i) = \frac{P(B_i) \cdot P_{B_i}(A)}{\sum_{j=1}^{n} P(B_j) \cdot P_{B_j}(A)}$$

This formula returns the probability of an outcome in the hypothesis that the event A has occured, or, more precisely, the probability that to occur the event A to be conditioned by the outcome B_i.

6. Define for a discrete (and finite) random variable the following numerical characteristics: mean value, variance and standard deviation.

***Answer*:**

Let ξ be a discrete (and finite) random variable with its probability distribution

$$\xi : \begin{pmatrix} x_1, x_2, \ldots, x_n \\ p_1, p_2, \ldots, p_n \end{pmatrix}, \sum_{i=1}^{n} p_i = 1, \; p_i = P(\xi = x_i)$$

Mean value: $M(\xi) = \sum_{i=1}^{n} x_i \, p_i$. The mean value represents a numerical value around which it's find a group of the values for this random variable.

Variance: $D^2(\xi) = \sigma^2 = M\left[(\xi - M(\xi))^2\right]$.

Standard deviation: $D(\xi) = \sigma = \sqrt{D^2(\xi)}$.

The variance and the standard deviation are indicators which explain the "scattering" of the values for a random variable, giving information on the concentration degree of the values around to its mean value.

7. Define the Laplace transform and write the formula for the derivative.

***Answer*:**

If *f* is an original function, then its Laplace transform is

$$(Lf)(s) = \int_0^{\infty} f(t) e^{-st} dt$$

Image of the derivative: $(Lf')(s) = s(Lf)(s) - f(0_+)$.

8. Define the Z transform (the discrete Laplace transform) and calculate its image for the unit-step signal.

***Answer*:**

If {*fn*} is an original sequence, then its *Z* transform is:

$$Z(f_n)(z) = \sum_{n=1}^{\infty} f_n z^{-n}.$$

For the unit-step signal

$$\sigma_n = \begin{cases} 0, & n < 0, \\ 1, & \mathrm{n} \geq 0, \end{cases} \qquad \mathrm{n} \in \square$$

its *Z* transform is

$$Z(\sigma_n)(z) = \sum_{n=1}^{\infty} z^{-n} = \frac{1}{1-\frac{1}{z}} = \frac{z}{z-1}, \quad \text{for} \quad |z| < 1.$$

9. Polar, cylindrical and spherical coordinate systems.

***Answer*:**

The conversion between the Cartesian coordinates (*x*, *y*) of a point in the plane and the polar coordinates (ρ, ϕ) of the same point is given by the relations :

$$\begin{cases} x = \rho\cos\phi \\ y = \rho\sin\phi \end{cases},$$

where $\rho \in [0, \infty)$, $\phi \in [0, 2\pi)$.

The conversion between the Cartesian coordinates (*x, y, z*) of a point in three-dimensional space and the cylindrical coordinates (ρ, ϕ, z) of the same point is given by the relations :

$$\begin{cases} x = \rho\cos\phi \\ y = \rho\sin\phi \\ z = z \end{cases},$$

where $\rho \in [0, \infty)$, $\phi \in [0, 2\pi)$, $\mathrm{z} \in \mathbf{R}$.

The conversion between the Cartesian coordinates (*x, y, z*) of a point in three-dimensional space and the spherical coordinates (ρ, ϕ, θ) of the same point is given by the relations :

$$\begin{cases} x = \rho\cos\phi\sin\theta \\ y = \rho\sin\phi\sin\theta \\ z = \rho\cos\theta \end{cases},$$

where $\rho \in [0, \infty)$, $\phi \in [0, 2\pi)$, $\theta \in [0, \pi]$.

10. Physical and geometrical magnitudes calculated by integrals. Formula for the flux of a vector field.

***Answer*:**

Area of a plane domain, volume of a body, mass, centre of gravity, moments of inertia, the work of a field of force.

Let S be a smooth surface and let $\vec{v} = P\vec{i} + Q\vec{j} + R\vec{k}$ be a continuous vector field on S. The flux of the vector field $\vec{v}$ across the surface S oriented by the normal vector $\vec{n} = (\cos\alpha)\vec{i} + (\cos\beta)\vec{j} + (\cos\gamma)\vec{k}$ is:

$$\iint_S (\vec{v}\vec{n})dS = \iint_S (P\cos\alpha + Q\cos\beta + R\cos\gamma)dS .$$

11. Derivative with respect to a versor of a real function. Gradient, divergence and curl.

***Answer*:**

Let $f : D \subset \mathbf{R} \to \mathbf{R}$ be a scalar field, let $\vec{s} \in \mathbf{R}^3$, ||s||=1, be a versor and $\vec{a} \in D$. The derivative of f in the direction of $\vec{s}$ at the point $\vec{a}$ is the limit (provided that it exists)

$$\lim_{t\to 0} \frac{1}{t}[f(\vec{a} + t\vec{s}) - f(\vec{a})] := \frac{\partial f}{\partial \vec{s}}(\vec{a})$$

The derivative $\frac{\partial f}{\partial \vec{s}}(\vec{a})$ characterizes the velocity variation of f with respect to $\vec{s}$ at the point $\vec{a}$. The gradient of f at $\vec{a}$ is defined by

$$gradf(\vec{a}) = \nabla f(\vec{a}) = \frac{\partial f}{\partial x}(\vec{a})\vec{i} + \frac{\partial f}{\partial y}(\vec{a})\vec{j} + \frac{\partial f}{\partial z}(\vec{a})\vec{k}$$

where Nabla is the operator of Hamilton: $\nabla = \frac{\partial}{\partial x}\vec{i} + \frac{\partial}{\partial y}\vec{j} + \frac{\partial}{\partial z}\vec{k}$.

It can be proved that $\frac{\partial f}{\partial \vec{s}}(\vec{a}) = \vec{s} \cdot \nabla f(\vec{a})$, that is the directional derivative of f at $\vec{a}$ in the direction $\vec{s}$ is equal to the dot product between the gradient of f and $\vec{s}$.

From here it follows that the gradient direction of a scalar field is the direction of maximum value of that field, that is the field has the fastest variation.

Let $\vec{v} : U \to \mathbf{R}$ be a vector field defined on an open set $U \subset \mathbf{R}^3$, $\vec{v} = (P, Q, R)$. The divergence of the field $\vec{v}$ at a current point is the scalar (number)

$$div\vec{v} = \frac{\partial P}{\partial x} + \frac{\partial Q}{\partial y} + \frac{\partial R}{\partial z}.$$

The curl of the field $\vec{v}$ at a current point is the vector

$$curl\vec{v} = \nabla f(\vec{a}) = \left(\frac{\partial R}{\partial y} - \frac{\partial Q}{\partial z}\right)\vec{i} + \left(\frac{\partial P}{\partial z} - \frac{\partial R}{\partial x}\right)\vec{j} + \left(\frac{\partial Q}{\partial x} - \frac{\partial P}{\partial y}\right)\vec{k}.$$

12. Write the Fourier series and the Fourier coefficients for a continuous periodic signal.

***Answer*:** Let $f : \mathbf{R} \to \mathbf{R}$ be an integrable and periodic function having the period T and $\omega = \frac{2\pi}{T}$. The Fourier coefficients are:

$$a_n = \frac{2}{T}\int_0^T f(t)\cos(n\omega t)dt, \quad n = 0,1,...$$

$$b_n = \frac{2}{T}\int_0^T f(t)\sin(n\omega t)dt, \quad n = 1,2,...$$

The Fourier series associated to f is:

$$\frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos(n\omega x) + b_n \sin(n\omega x).$$

13. Define the Fourier transform. The Fourier inverting formula.

***Answer*:**

The Fourier transform of an absolutely integrable function $f : \mathbf{R} \to \mathbf{C}$ is:

$$\hat{f}(\omega) = \int_R f(t) e^{-it\omega} dt.$$

The Fourier inverting formula is

$$f(t) = \frac{1}{2\pi}\int_R \hat{f}(\omega) e^{it\omega} d\omega.$$

14. Write the filtering formula and the Fourier transform for the unit impulse.

***Answer*:**

The filtering formula is: $\delta(x - x_0) = \delta_{x_0}$, where δ is the Dirac's distribution.

The Fourier transform is $\hat{\delta} = 1$.

15. Solve the Cauchy-Problem

$$\begin{cases} x'(t) = a(t)x(t) \\ x(t_0) = x_0 \end{cases}$$

where a is a continuous function.

Answer:

The given equation can be rewritten as

$$\frac{x'(s)}{x(s)} = a(s).$$

Integrating between t_0 and t, we obtain

$$\ln x(t) - \ln x(t_0) = \int_{t_0}^{t} a(s)ds \Leftrightarrow \ln \frac{x(t)}{x(t_0)} = \int_{t_0}^{t} a(s)ds.$$

Thus, the sought-for solution is

$$x(t) = x_o e^{\int_{t_0}^{t} a(s)ds} \quad .$$

Physics

1. Definition of mechanical energy

Answer: The general form of the definition for mechanical energy is: $E_{mech} = K + PE$
Where:
PE refers to the total potential energy of the system, including all types of potential energy; [J]
K refers to the sum of the kinetic energies of all particles in the system, [J]
E_{mech} is the total mechanic energy ; [J]

2. Definition of the kinetic energy

Answer: The kinetic energy *K* of an object of mass m moving with a speed v is defined as $K = ½ (mv^2)$
K is the kinetic energy of the moving object [J]
m is the mass of the moving object [kg]
v is the speed of the object [m/s]

3. Definition of work

Answer: The work *W* done on a system by an external agent exerting a constant force on the system is the product of the magnitude *F* of the force, the magnitude Δr of the displacement of the point of application of the force, and cos θ,
where θ is the angle between the force and displacement vectors. The work is a scalar quantity.
W is the work [J]
F is the constant external force acting on the system [N]
Δr is the magnitude of the displacement, [m]
The work done by a variable net force is

$$\sum W = W_{\text{net}} = \int \left(\sum \vec{\mathbf{F}} \right) \cdot d\vec{\mathbf{r}}$$

where the integral is calculated over the path that the particle takes through space.

4. Definition of potential energy

Answer: The expression of potential energy, in linear systems, is a function of position (relative position). The corresponding force is also a function of position.
The gravitational potential energy PE is the energy that an object of mass *m* has by virtue of its position relative to the surface of the earth. That position is measured by the height *h* of the object relative to an arbitrary zero level: $PE = mgh$
PE is the gravitational potential energy [J]
m is the mass [kg]
g is the gravitational acceleration [m/s^2]
h is the height [m]

5. Definition of (mechanical) power

Answer: Power is the rate at which energy is expended or converted to another form.
Mechanically, it is the rate at which work is done. Power is work done per unit time.
Average power: P = W/t = work[J]/time[s] .
SI Unit for power is the watt: 1W=1J/1s

6. Definition of heat

Answer: Heat is energy that flows from a higher-temperature object to a lower-temperature object because of the difference in temperatures. The substance has internal energy, not heat. The word "heat" is used only when referring to the energy actually in transit from hot to cold.
SI Unit of Heat: joule (J)

7. Conservation of mechanical energy

Answer: For an isolated system the energy in the system is conserved and the sum of the kinetic and potential energies remains constant. KE + PE = constant
The total mechanical energy, E_{mech} = KE + PE of an object remains constant as the object moves, provided that the net work done by external nonconservative forces is zero, $W_{nc}=0$.

8. Conservation of linear momentum (impulse) for an isolated system

Answer: The linear momentum of a particle or an object that can be modeled as a particle of mass *m* moving with a velocity $\vec{v}$ is defined to be the product of the mass and velocity: $\vec{p} = m\vec{v}$.
The total linear momentum of an isolated (net external force equal to zero) system remains constant.

$$\sum \vec{F} = \frac{d\bar{p}}{dt} = 0\,; \qquad \vec{p}_{tot} = \text{constant}$$

9. The conservation of the angular momentum

Answer: The instantaneous angular momentum of the particle relative to the origin *O* is defined by the vector $\bar{L}$
product of its instantaneous position vector $\bar{r}$ and the instantaneous linear momentum $\bar{p}$.

$$\bar{L} = \bar{r} \times \bar{p}$$

The total angular momentum of a system is conserved if the net external torque acting on the system is zero.

$\bar{M}_{ext} = \bar{r} \times \bar{F}_{ext}$ $\qquad$ $\bar{M} = \frac{d\bar{L}}{dt}$ $\qquad$ External $\bar{M} = 0, \rightarrow \frac{d\bar{L}}{dt} = 0, \rightarrow \bar{L} = \text{constant}$

10. The Hooke's law

Answer: The force of an elastic system (spring), inside the limits of linearity (elasticity) is given by

$$\vec{F} = -k\vec{x}$$

Where *x* is the displacement of the spring's end from its equilibrium position (a distance, in SI units: m);

F is the restoring force exerted by the material (in SI units: N or $kgms^{-2}$); and
k is a constant called the *rate* or *spring constant* (in SI units: $N \cdot m^{-1}$ or kgs^{-2}).

For an elastic bar: $$\Delta l = \frac{F \cdot l_0}{S \cdot E}$$

Where F is the force [N] , l_0 is the initial length of the bar [m], S is the cross section of the bar [m^2] and E is the Young' module (elasticity) of the material of the bar [N/m^2].

11. Archimedes's law

Answer: The apparent loss in weight of a body immersed in a fluid is equal to the weight of the displaced fluid
Or: a body immersed in a fluid is pushed up, in the vertical direction, with a force equal to the weight of the volume of the displaced fluid.

12. The law of absorption of waves

A: In a homogenous dissipative media the intensity of plane waves reduces exponentially with the distance

$$I = I_0 e^{-k x}$$

where I_0 is the intensity of the penetrating wave, I is the intensity of the wave at distance x, and k is the absorption coefficient.
The absorption coefficient is a characteristic of the medium, depending also on the wave length of the incident wave
The intensity „I" of the wave is numerically equal to the energy carried by the wave in a second, trough the surface normal (orthogonal on the wave direction of propagation.

13. The reflection laws

Answer: The incident ray, the reflected ray, and the normal to the surface all lie in the same plane, and
the angle of reflection equals the angle of incidence .

14. The refraction laws

Answer: When light travels from a material with refractive index n_1 into a material with refractive index n_2, the refracted ray, the incident ray, and the normal to the interface between the materials all lie in the same plane. The angle of refraction is related to the angle of incidence by $n_1 \cdot \sin\theta_1 = n_2 \cdot \sin\theta_2$.

The index of refraction *n* of a material is the ratio of the speed *c* of light in a vacuum to the speed *v* of light in the material.

15. Coulomb's law

Answer: The magnitude F of the electrostatic force exerted by one point charge q_1 on another point charge q_2 is directly proportional to the magnitudes $|\ q_1\ |$ and $|\ q_2\ |$ of the charges and inversely proportional to the square of the distance r between them.

$$F = \frac{q_1 \cdot q_2}{4\pi\varepsilon} \cdot \frac{1}{r^2}$$

The electrostatic force is directed along the line joining the charges, and it is attractive if the charges have unlike signs and repulsive if the charges have like signs.

Measuring Units

of the International System of Units

1. ***Specify the SI unit and its symbol for mass. Specify the multiplier and its symbol for micro (example: atto = 10^{-18}, a).***

   The SI unit for mass is the kilogram. Its symbol is kg. The multiplier for micro is 10^{-6}. Its symbol is μ.

2. ***Specify the SI unit and its symbol for length. Specify the multiplier and its symbol for milli (example: atto = 10^{-18}, a).***

   The SI unit for length is the metre. Its symbol is m. The multiplier for milli is 10^{-3}. Its symbol is m.

3. ***Specify the SI unit and its symbol for time. Specify the multiplier and its symbol for micro (example: atto = 10^{-18}, a).***

   The SI unit for time is the second. Its symbol is s. The multiplier for micro is 10^{-6}. Its symbol is μ.

4. ***Specify the SI unit and its symbol for electrical current. Specify the multiplier and its symbol for milli (example: atto = 10^{-18}, a).***

   The SI unit for electrical current is the ampere. Its symbol is A. The multiplier for milli is 10^{-3}. Its symbol is m.

5. ***Specify the SI unit and its symbol for angular velocity. Specify the multiplier and its symbol for kilo (example: atto = 10^{-18}, a).***

   The SI unit for angular velocity is the radian per second. Its symbol is rad/s. The multiplier for kilo is 10^{3}. Its symbol is k.

6. ***Specify the SI unit and its symbol for frequency. Specify the multiplier and its symbol for tera (example: atto = 10^{-18}, a).***

   The SI unit for frequency is the hertz. Its symbol is Hz. The multiplier for tera is 10^{12}. Its symbol is T.

7. ***Specify the SI unit and its symbol for energy, work and heat. Specify the multiplier and its symbol for mega (example: atto = 10^{-18}, a).***

   The SI unit for energy, work and heat is the joule. Its symbol is J. The multiplier for mega is 10^{6}. Its symbol is M.

8. ***Specify the SI unit and its symbol for power and radiant flux. Specify the multiplier and its symbol for giga (example: atto = 10^{-18}, a).***

The SI unit for power and radiant flux is the watt. Its symbol is W. The multiplier for giga is 10^9. Its symbol is G.

9. Specify the SI unit and its symbol for electrical charge and quantity of electricity. Specify the multiplier and its symbol for femto (example: atto = 10^{-18}, a).

The SI unit for electrical charge and quantity of electricity is the coulomb. Its symbol is C. The multiplier for femto is 10^{-15}. Its symbol is f.

10. Specify the SI unit and its symbol for voltage, electrical potential difference and electromotive force. Specify the multiplier and its symbol for nano (example: atto = 10^{-18}, a).

The SI unit for voltage, electrical potential difference and electromotive force is the volt. Its symbol is V. The multiplier for nano is 10^{-9}. Its symbol is n.

11. Specify the SI unit and its symbol for electrical field strength. Specify the multiplier and its symbol for mega (example: atto = 10^{-18}, a).

The SI unit for electrical field strength is the volt per metre. Its symbol is V/m. The multiplier for mega is 10^6. Its symbol is M.

12. Specify the SI unit and its symbol for electric resistance, impedance and reactance. Specify the multiplier and its symbol for kilo (example: atto = 10^{-18}, a).

The SI unit for electric resistance, impedance and reactance is the ohm. Its symbol is Ω. The multiplier for kilo is 10^3. Its symbol is k.

13. Specify the SI unit and its symbol for electrical conductance. Specify the multiplier and its symbol for kilo (example: atto = 10^{-18}, a).

The SI unit for electrical conductance is the siemens. Its symbol is S. The multiplier for kilo is 10^3. Its symbol is k.

14. Specify the SI unit and its symbol for electric capacitance. Specify the multiplier and its symbol for pico (example: atto = 10^{-18}, a).

The SI unit for electric capacitance is the farad. Its symbol is F. The multiplier for pico is 10^{-12}. Its symbol is p.

15. Specify the SI unit and its symbol for inductance. Specify the multiplier and its symbol for milli (example: atto = 10^{-18}, a).

The SI unit for inductance is the henry. Its symbol is H. The multiplier for milli is 10^{-3}. Its symbol is m.

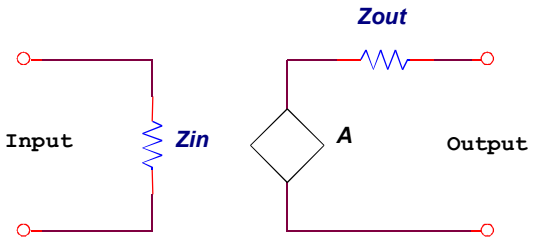
Electronic Circuits

1. *Demonstrate the optimum input and output impedance for a voltage amplifier.*

2011 EC (c 01).ppt / slides 8,9

Amplifiers fundamental properties

- *Gain*
- *Input impedance*
- *Output impedance*



General amplifier model

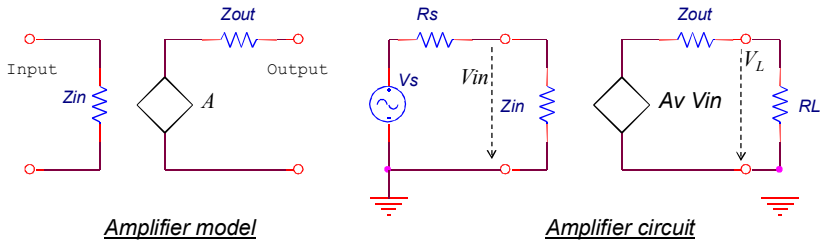
- There are three types of gain:

voltage gain (A_V),
current gain (A_I),
power gain (A_P).

$$A_V = \frac{V_{OUT}}{V_{IN}} \qquad A_I = \frac{I_{OUT}}{I_{IN}} \qquad A_P = \frac{P_{OUT}}{P_{IN}}$$

- The gain of a circuit is determined by its component values !!!
- When the **gain** of a circuit has been calculated, it can be used to determine the **output** of the circuit for **a specified input**

Ex: Voltage amplifier circuit



Amplifier model *Amplifier circuit*

- At the circuit input and output there are 2 voltage dividers:

$$v_{IN} = v_S \frac{Z_{IN}}{R_S + Z_{IN}} \qquad v_L = v_{OUT} \frac{R_L}{Z_{OUT} + R_L} \qquad \text{where} \quad v_{OUT} = A_V v_{IN}$$

- Since $v_{IN} < v_S$ and $v_L < v_{OUT}$

=> The *effective voltage gain* of a circuit is lower than the calculated voltage gain of the amplifier itself.

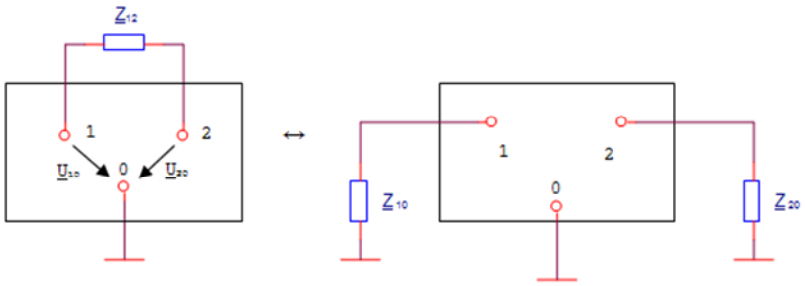
To neglect the input and output voltage drop we must have :

***[Infinite gain], Infinite input impedance, Zero output impedance* !!!**

2. ***Explain Miller effect and theorem and its utility for high frequency analysis.***
2011 EC (c 03+04).ppt /slides 37-38, seminar nr.2.doc

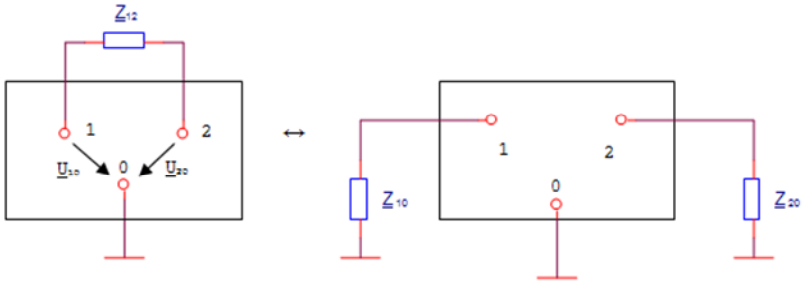
Miller Effect

An impedance Z_{12} connected from the input of an amplifier to the output can be replaced by an impedance across the input terminals (Z_{10}) and impedance across the output terminals (Z_{20}).



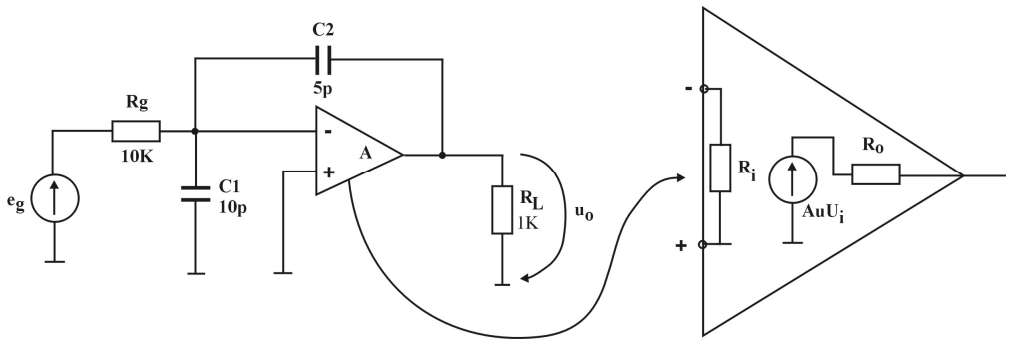
Miller Effect

An impedance Z_{12} connected from the input of an amplifier to the output can be replaced by an impedance across the input terminals (Z_{10}) and impedance across the output terminals (Z_{20}).



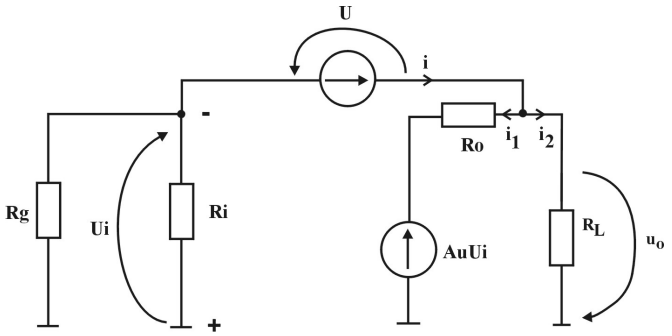
Example: For the following circuit, we consider the amplifier's parameters:

$A_u = 10^2$, $R_i = 1M\Omega$, $R_0 = 1K$.



Compute high cut of limit frequency of the circuit, using Miller's theorem

Answer:



$$f_{p_1} = \frac{1}{2\pi(C_{10} + C_1)R_g \| R_i} = 60KHz \quad f_{p_2} = \frac{1}{2\pi(C_{20})R_g \| R_i} = 64KHz$$

,

$$C_{10} = C_2(1-K),\ C_{20} = C_2(1-\frac{1}{K}),\ \ K = \frac{U_o}{U_i} = \frac{A_u U_i \dfrac{R_L}{R_o + R_L}}{U_i} = A_u \frac{R_L}{R_o + R_L}$$

$f_{p2} >> f_{p1} \rightarrow$ $\qquad f_i \cong f_{p1} = 60\text{KHz}$

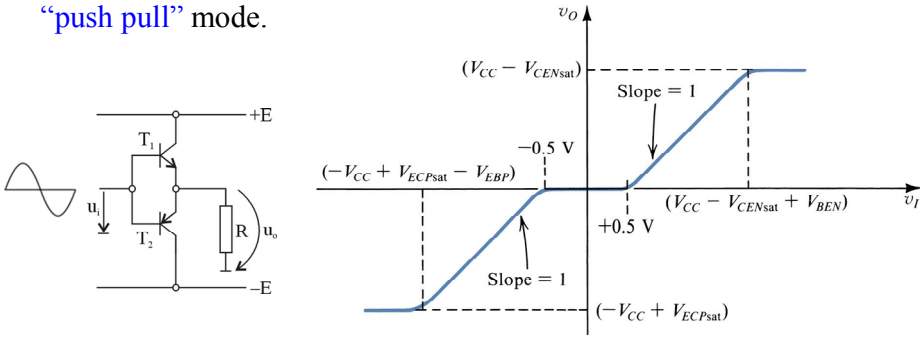
3. *Which amplifier class is known for its crossover distortions? Explain the root cause and ways of improvement based on a simplified schematic and is transfer characteristic.*

2011 EC (c 05).ppt / slides 22-24, 37

Class B - output stage circuit

Named also *Complementary-symmetry amplifier*

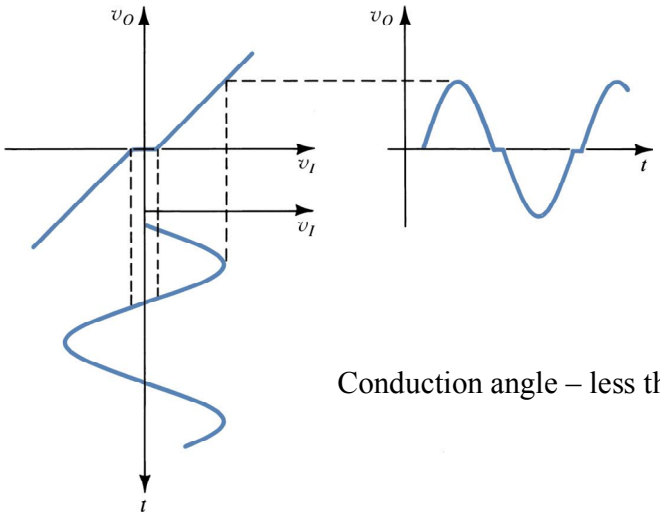
= 2 complementary BJT's used as emitter followers, working in "push pull" mode.



Advantage: good efficiency – up to 78.5% (in DC mode – no current sink from supply)

Drawback: Crossover distortion

Class B – crossover distortion

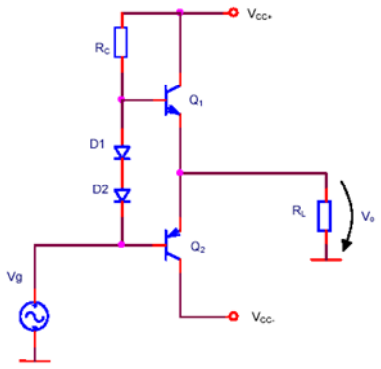


Conduction angle – less than ½ T

=> crossover distortion between the "halves" of the signal

Class B biasing

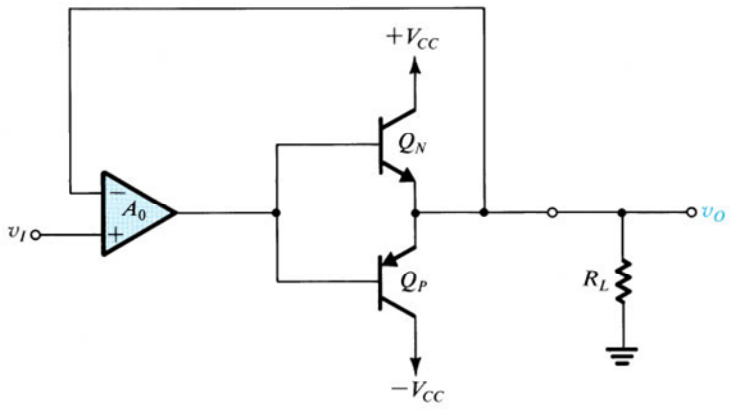
Biasing must provide V(B1)- V(B2) to keep Q1 and Q2 off, but close to conduction => lower crossover distortion



BJT 's can be biased using 2 diodes or a "V_{BE} multiplier" circuit => constant voltage drop between Q1 and Q2 bases

Opamp Implementation

Op amp connected in a negative-feedback loop to reduce crossover distortion

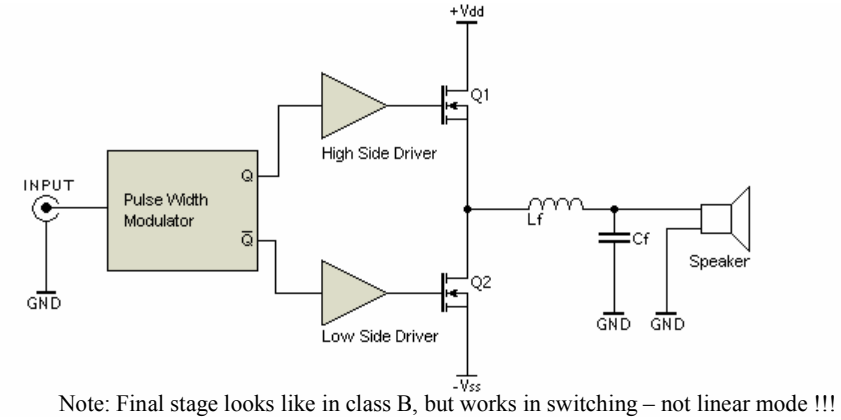


4. Describe half bridge class D amplifiers topology, block schematic and principle of operation.

2011 EC (c 06).ppt / slides 5-7

Class D – (half bridge) simplified circuit

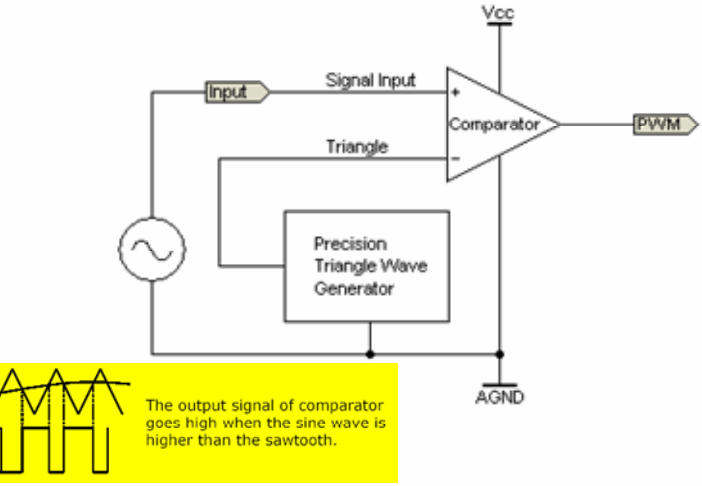
– operation is switching, hence the term *switching power amplifier*
– output devices are rapidly switched on and off at least twice for each cycle
– the output devices are either completely on or completely off so theoretically they do not dissipate any power



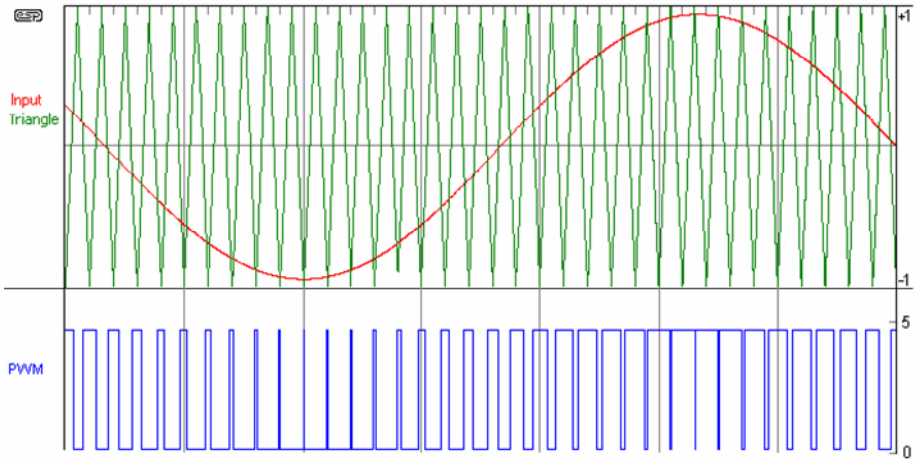
Note: Final stage looks like in class B, but works in switching – not linear mode !!!

Class D - PWM signal generation

- The input signal is compared with a triangle signal resulting in a PWM (Pulse width modulation) signal



Class D – PWM waveforms

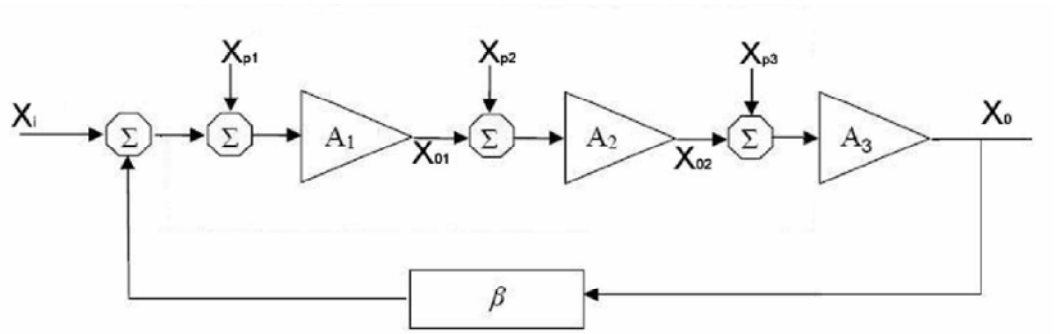


- Usually 150KHz to 250Khz switching freq. is used
- The LC LPF provide at the output the mean value of the PWM signal - same shape as the Input signal

5. *Using formula show the most unwanted occurrence place for an external perturbation in a multistage amplifier sing a gobal negative feedback loop*

2011 EC (c 07).ppt/ slide 11

Perturbation influence in Feedback Amps



$$\begin{cases} x_0 = (x_{02} + x_{p3})A_3 \\ x_{02} = (x_{01} + x_{p2})A_2 \\ x_0 = (x_\Sigma + x_{p1})A_1 \\ x_\Sigma = x_i - x_r = x_i - \beta x_0 \end{cases}$$

$$x_0 = (((x_i - \beta x_0 + x_{p1})A_1 + x_{p2})A_2 + x_{p3})A_3$$

Perturbations are reduced as they are closer to output

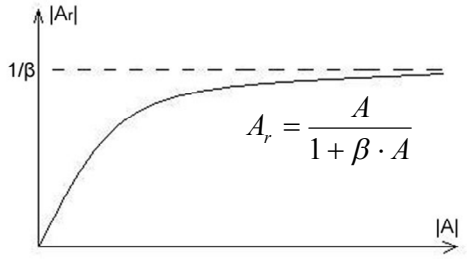
$$\Rightarrow x_0 = x_i \frac{A_1A_2A_3}{1+\beta A_1A_2A_3} + x_{p1}\frac{A_1A_2A_3}{1+\beta A_1A_2A_3} + x_{p2}\frac{A_2A_3}{1+\beta A_1A_2A_3} + x_{p3}\frac{A_3}{1+\beta A_1A_2A_3}$$

6. *Demonstrate bandwidth extension for an amplifier when a negative feedback is applied.*

2011 EC (c 07).ppt /slides 5-7

Feedback effect over gain

- For amplifiers with feedback we can assume that the



If nonfeedback amplifier has : $\Delta A / A$

$$\Delta A_r / A_r \overset{???}{\Longleftrightarrow} \Delta A / A$$

At small variations :

$$\Delta A_r \cong \frac{1+\beta A - A\beta}{(1+\beta A)^2} \cdot \Delta A = \frac{1}{(1+\beta A)^2} \cdot \Delta A = \frac{A}{1+\beta A} \cdot \frac{1}{1+\beta A} \cdot \frac{\Delta A}{A} \Rightarrow$$

$$\frac{\Delta A_r}{A_r} \cong \frac{\Delta A}{A} \cdot \frac{1}{1+\beta A} = \frac{\Delta A}{A} \cdot \frac{1}{F}$$

F times improvement !!!

Influence of the feedback on freq. response

If $A(j\omega) = \frac{P(j\omega)}{Q(j\omega)} \cdot A_0$ and $\beta = \beta_0$ a real number,

Then: $A_r(j\omega) = \frac{\frac{P}{Q} \cdot A_0}{1 + \beta_0 \frac{P}{Q} \cdot A_0} = \frac{PA_0}{Q + \beta_0 PA_0}$

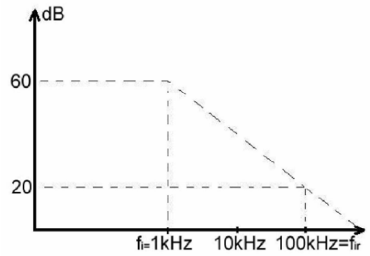
only the poles are shifted

$$\text{EX 1}: A(j\omega) = \frac{A_0}{1 + j\frac{f}{f_i}} \qquad \beta = \beta_0$$

$$A_r(j\omega) = \frac{\frac{A_0}{1 + j\frac{f}{f_i}}}{1 + \frac{\beta_0 A_0}{1 + j\frac{f}{f_i}}} = \frac{A_0}{1 + \beta_0 A_0 + j\frac{f}{f_i}} = \frac{A_0}{1 + \beta_0 A_0} \cdot \frac{1}{1 + j\frac{f}{f_i(1 + \beta_0 A_0)}} = A_{ro} \cdot \frac{1}{1 + j\frac{f}{f_{ir}}}$$

where $A_{r0} = \frac{A_0}{1 + \beta_0 A_0}$ & $f_{ir} = f_i(1 + \beta_0 A_0)$

Then: $A_r = \frac{A}{F}$; $f_{ir} = f_i F$; $A_r \cdot f_{ir} = A \cdot f_i$



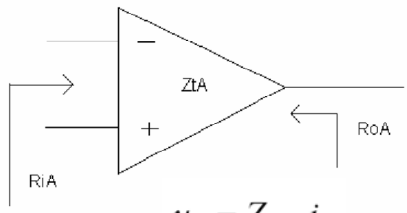
Note: only if circuit still behave linear !!!

7. *Show input and output resistance change for an amplifier when a shunt-shunt feedback is applied. Justify with formulas.*

2011 EC (c 08).ppt / slides 7,8,10

Shunt Shunt Negative Feedback

$$\begin{cases} u_0 = Z_t \cdot \dfrac{R_L \| R_{if}}{R_L \| R_{if} + R_0} \cdot i_i \\ i_i = i_{iA} \cdot \dfrac{R_g \| R_{of}}{R_g \| R_{of} + R_i} \\ i_{iA} = i_g - i_r = i_g - \beta u_0 \end{cases}$$



$$u_0 = Z_{tA} \cdot i_{iA}$$

$$Z_{tA} = \frac{u_0}{i_g}\Big|_{\beta=0}$$

$$\beta = \frac{i_r}{u_0}\Big|_{u_i=0}$$

-Obtained by separating feedback network

$$u_0 = \underbrace{Z_t \cdot \frac{R_L \| R_{if}}{R_L \| R_{if} + R_0} \cdot \frac{R_g \| R_{of}}{R_g \| R_{of} + R_i}}_{Z_{tA}} \cdot i_{iA}$$

Z_{tA}

Transfer impedance of the amp. with influences included and no feedback

Shunt Shunt Negative Feedback

$$Z_{tA} = Z_{tr}\,|\,_{=0}$$

$$u_0 = Z_{tA} \cdot i_{iA} = Z_{tA}(i_g - i_r) = Z_{tA}(i_g - \beta u_0)$$

$$\Rightarrow \quad \boxed{Z_{tr} = \frac{u_0}{i_g} = \frac{Z_{tA}}{1 + \beta \cdot Z_{tA}}}$$

$$R_{ir} = \frac{u_i}{i_g}$$

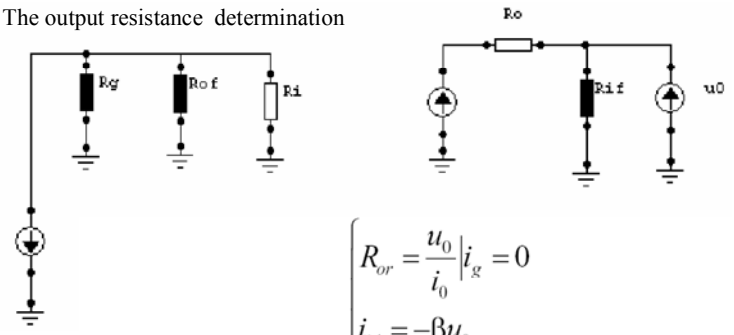
$$i_g = i_r + i_{iA} = \beta u_0 + \underbrace{\frac{u_i}{R_g \| R_{of} \| R_i}}_{R_{iA}} = \beta u_0 + \frac{u_i}{R_{iA}} = \beta \cdot Z_{tA} \cdot i_{iA} + \frac{u_i}{R_{iA}}$$

$$i_g = \beta \cdot Z_{tA} \cdot \frac{u_i}{R_{iA}} + \frac{u_i}{R_{iA}} \quad \Rightarrow \quad \boxed{R_{ir} = \frac{u_i}{i_g} = \frac{R_{iA}}{1 + \beta \cdot Z_{tA}}}$$

Small value, because ig split also to the feedback network.

Shunt Shunt Negative Feedback

The output resistance determination



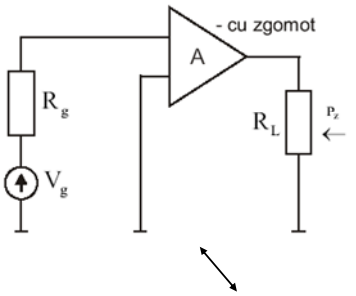
$$R_{or} = \frac{u_0}{i_0}\,|\,i_g=0$$

$$\begin{cases} R_{or} = \dfrac{u_0}{i_0}\Big|_{i_g = 0} \\ i_{iA} = -\beta u_0 \\ i_0 = \dfrac{u_0}{R_{if}} + \dfrac{u_0 - Z_t \cdot i_i}{R_0} \Rightarrow i_0 = \dfrac{u_0}{R_{if}} + \dfrac{u_0(1+\beta Z_t)}{R_0} \\ i_i = i_{iA} \cdot \dfrac{R_g \| R_{of}}{R_g \| R_{of} + R_i} \end{cases}$$

8. *Draw noise equivalent schematic of an amplifier and define noise factor F.*

2011 EC (c 11).ppt / slides 17, 18, 19

Noise model for an Amplifier

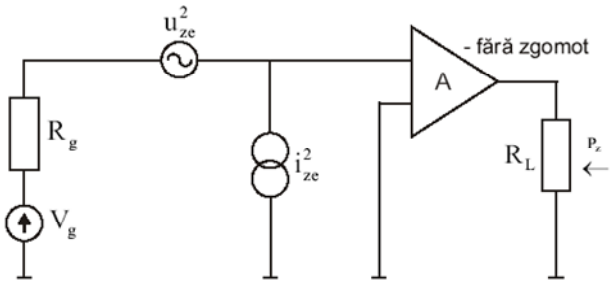


If the noise sources are uncorrelated, noise at output:

$$P_z = \sum_{k=1}^{n} P_{zk}$$

$$P_{zk} \rightarrow i_{zk}^2, u_{zk}^2 \rightarrow R_L$$

$u_{zet}^2 = u_{ze}^2 + i_{ze}^2 \cdot R_g^2$ Total noise voltage



2011 Electronic Circuits Course Slide 17

Noise figure (factor)

- Compare noise produced by the amp. with the noise produced by the generator Rg

$$F = \frac{SNR_{in}}{SNR_{out}}$$ SNR – signal to noise ratio

$$F \overset{def}{=} \frac{\text{Puterea totală de zgomot de la ieșire}}{\text{Puterea de zgomot datorată generatorului}}$$

$$F_{dB} = 10 \lg F$$

$$F_{dB} = 10 \lg \frac{P_{zg} + P_{zA}}{P_{zg}} \text{ unde } P_{zg} = \frac{u_{zg}^2}{(R_g + R_i)^2} \cdot R_i^2$$

$$P_{zA} = \frac{u_{ze}^2}{(R_g + R_i)^2} \cdot R_i^2 + \frac{i_{ze}^2 \cdot R_g^2}{(R_g + R_i)^2} \cdot R_i^2$$

$$F_{dB} = 10 \lg \left(1 + \frac{u_{ze}^2 + i_{ze}^2 \cdot R_g^2}{u_{zR_g}^2} \right) \qquad u_{zR_g}^2 = 4kTR_g \cdot \Delta f$$

2011 Electronic Circuits Course Slide 18

9. *Explain dominant pole (lag) compensation method. How is related dominant pole frequency to gain unity frequency f_{0dB}. Show practical implementation.*

2011 EC (c 10).ppt / slides 19-21

4.1 Dominant-pole compensation

It represents a very popular method, also called **lag compensation**. It consists in adding another pole in the open-loop transfer function - A(jω) - at a very low frequency, such that the loop-gain drops to unity by the time the phase reaches -180°:

$$A_C(j\omega) = A(j\omega)\frac{1}{1+j\dfrac{f}{f_d}}$$

$$f_d << \min(f_{pk})$$

where f_{pk} are the pole frequencies for A(jω).

A serious disadvantage of this compensation method is the resulting close-loop amplifier bandwidth, drastically reduced (fig. 4).

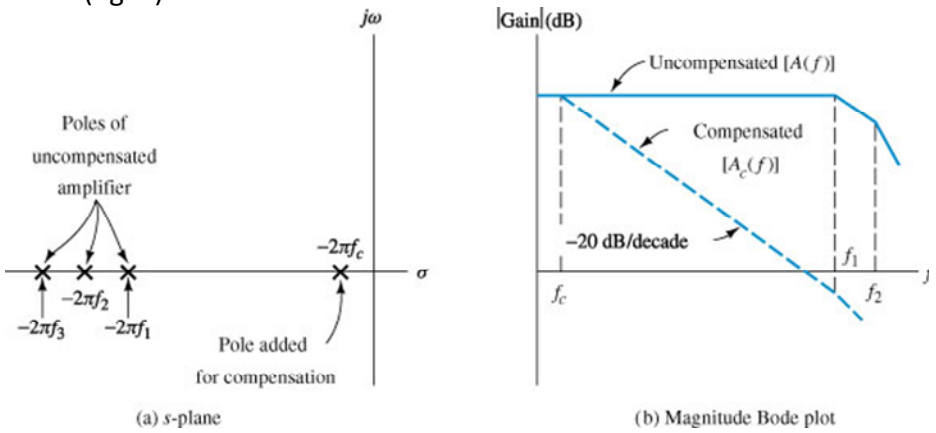


Fig. 4. Dominant-pole compensation.

It could be shown that knowing f_{0dB} is sufficient for computing f_d:

$$f_d = f_{0dB}\left|\frac{A_f}{A_0}\right|$$

where A_0 is the open-loop midband frequency gain.

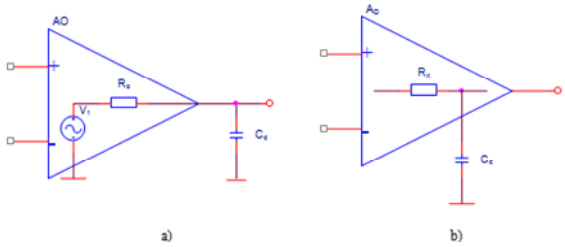


Fig. 5. Dominant-pole implementation.

10. Draw and characterize a Wien network and show how is connected to build a Wien oscillator. What are the conditions used to design feedback loops.

2011 EC (c 12,13).ppt / slides 18,11,19
2011 Sem 7.ppt

3.2 The Wien Bridge Oscillator

An oscillator circuit in which a balanced bridge is used as the feedback network

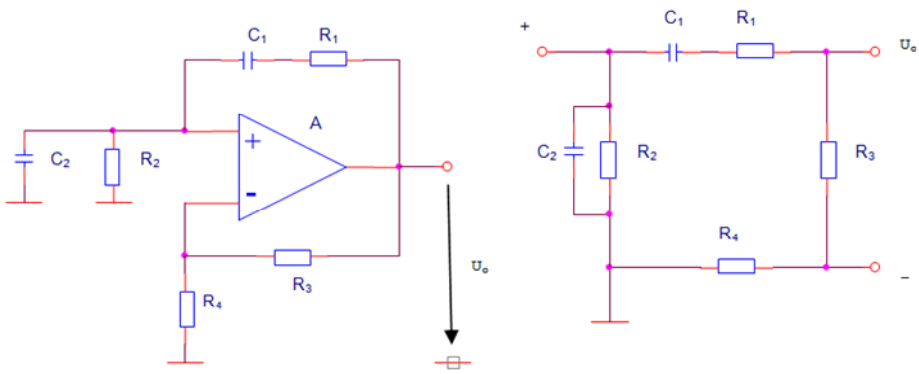


Fig. 4. a) A Wien bridge oscillator. b) The bridge network

Barkhausen Criterion.

- The condition for the feedback loop to provide sinusoidal oscillation of frequency ω is:

$$A(j\omega)\beta(j\omega) = 1 \Leftrightarrow$$

$$\begin{cases} \arg A(j\omega) + \arg \beta(j\omega) = 2k\pi & \text{phase criterion} \\ \left|A(j\omega)\right|\left|\beta(j\omega)\right| = 1 & \text{amplitude criterion.} \end{cases}$$

Amplitude criterion. $\left|\underline{A}_{ur}\right|\left|\underline{\beta}_{+}\right|_{\omega=\omega_0} = 1$

For negative feedback loop: $\underline{A}_{ur} = \dfrac{A_u}{1+\beta_- A_u} \cong \dfrac{1}{\beta_-}$

=> $\left|\underline{\beta}_{+}\right| = \left|\underline{\beta}_{-}\right|$

$$\beta_- = \frac{R_4}{R_3 + R_4}$$

$$\beta_+(j\omega) = \frac{1}{1 + \dfrac{R_1}{R_2} + \dfrac{C_2}{C_1} + j\left(\omega C_2 R_1 - \dfrac{1}{\omega C_1 R_2}\right)}$$

In order to obtain oscillations, **phase criterion** has to be satisfied:

$$\beta_+(j\omega_0) \in \Re \Rightarrow \omega_0 C_2 R_1 - \frac{1}{\omega_0 C_1 R_2} = 0;$$

$$\omega_0^2 = \frac{1}{R_1 C_1 R_2 C_2} \Rightarrow f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi\sqrt{R_1 C_1 R_2 C_2}}$$

$$\begin{cases} \arg\left[\beta_+(j\omega_0)\right] = 0 \\ \left|\beta_+(j\omega_0)\right| = \dfrac{1}{1 + \dfrac{R_1}{R_2} + \dfrac{C_2}{C_1}} \end{cases}$$

Digital Integrated Circuits

1. *Positive edge triggered D type flip-flop: draw a symbolic representation, the operating table and its associated waveforms*

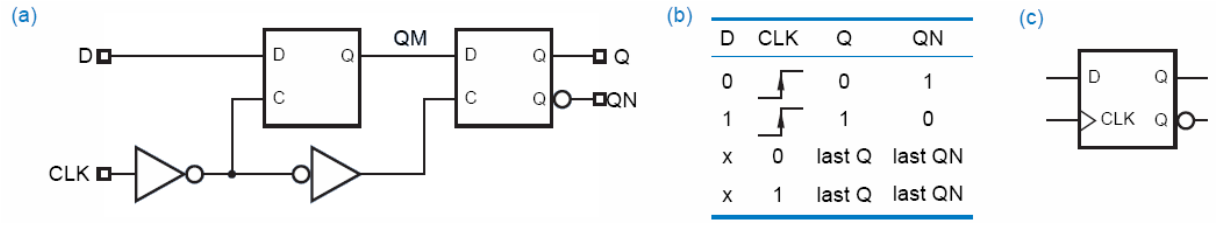
A positive-edge-triggered D flip-flop combines a pair of D latches, to create a circuit that samples its D input and changes its Q and QN outputs only at the rising edge of a controlling CLK signal.

The first latch is called the master; it is open and follows the input when CLK is 0. When CLK goes to 1, the master latch is closed and its output is transferred to the second latch, called the slave.

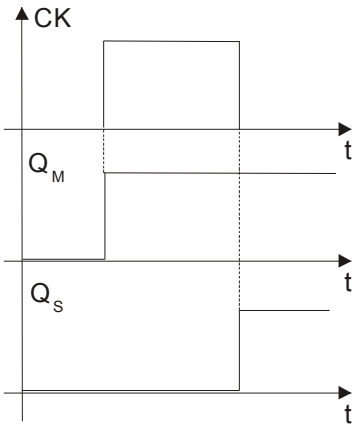
The slave latch is open all the while that CLK is 1, but changes only at the beginning of this interval, because the master is closed and unchanging during the rest of the interval.

Edge-Triggered D Flip-Flop

The triangle on the D flip-flop's CLK input indicates edge-triggered behavior, and is called a *dynamic-input indicator*.

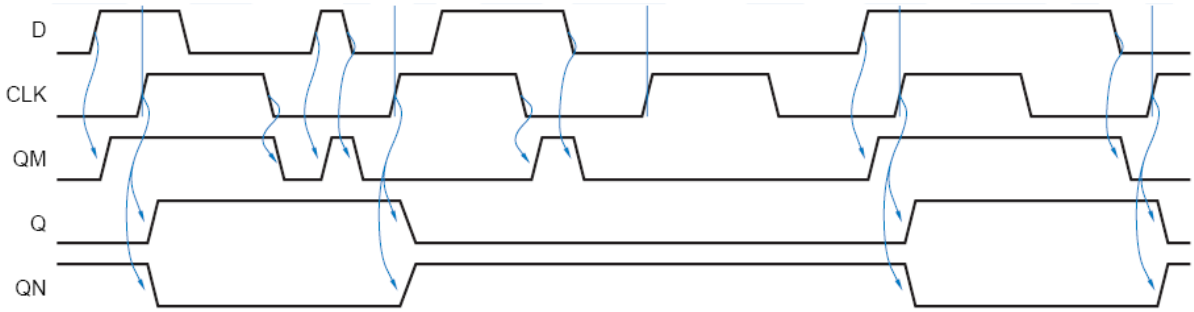


D	CLK	Q	QN
0	↑	0	1
1	↑	1	0
x	0	last Q	last QN
x	1	last Q	last QN

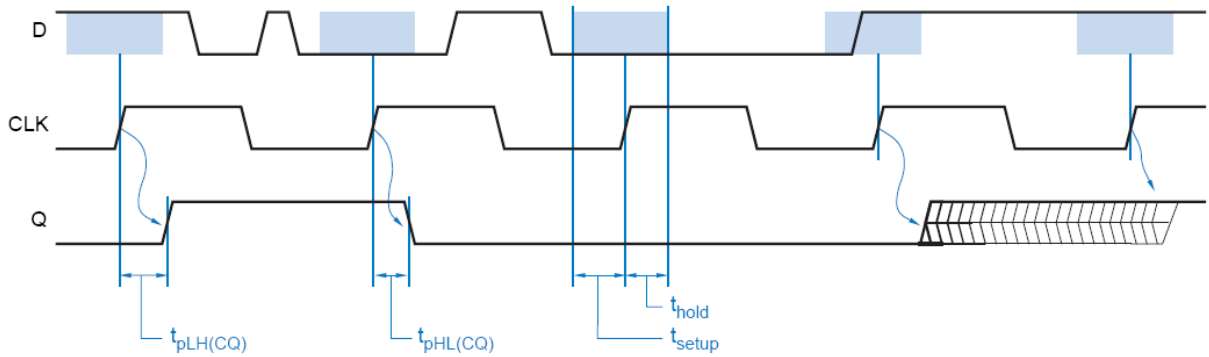


The QM signal shown is the output of the master latch.

Notice that QM changes only when CLK is 0. When CLK goes to 1, the current value of QM is transferred to Q, and QM is prevented from changing until CLK goes to 0 again.



Like a D latch, the edge-triggered D flip-flop has a setup and hold time window during which the D inputs must not change. This window occurs around the triggering edge of CLK, and is indicated by shaded color.



2. *Explain how a decoder can be used as a demultiplexer*

The 74x138 is a commercially available MSI 3-to-8 decoder whose gate-level circuit diagram and symbol are shown in Figure 5-37; its truth table is given in Table 5-7.

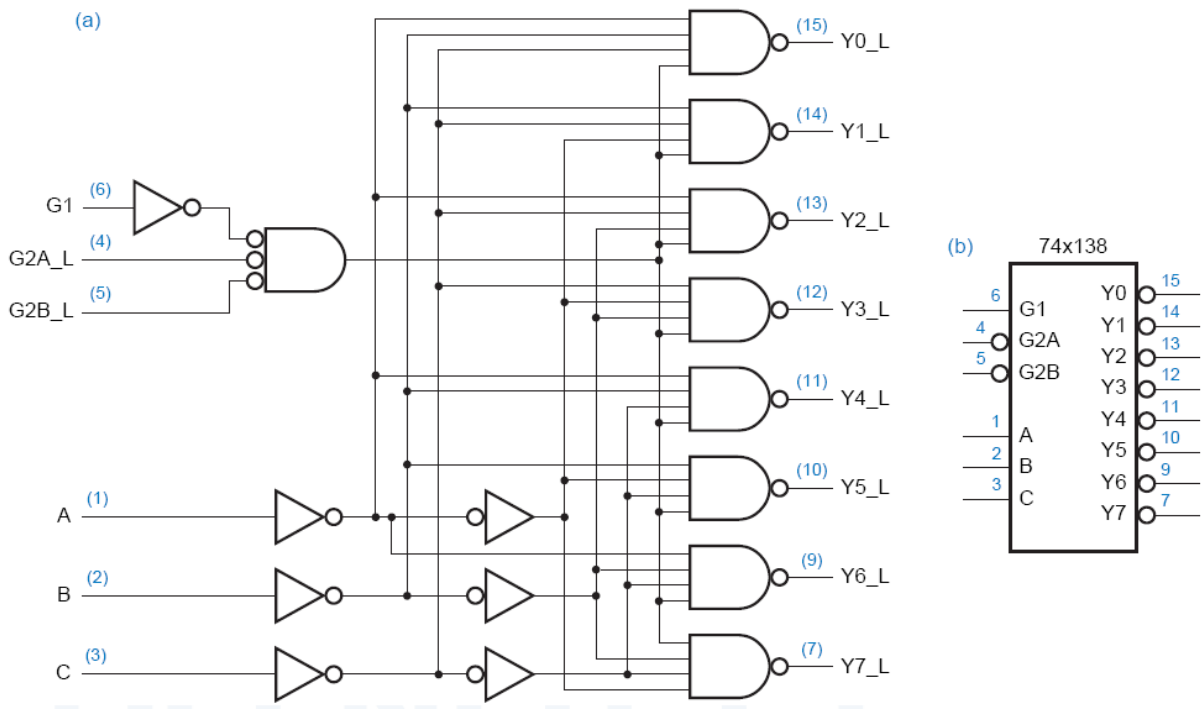


Figure 5-37

Like the 74x139, the 74x138 has active-low outputs, and it has three enable inputs (G1, nG2A, nG2B), all of which must be asserted for the selected output to be asserted.

Thus, we can easily write logic equations for an internal output signal such as Y5 in terms of the internal input signals:

However, because of the inversion bubbles, we have the following relations between internal and external signals:

$Y5 = G1.G2A.G2B \;.\; C \;.\; nB \;.\; A$

Enable Select

Therefore, if we're interested, we can write the following equation for the external output signal Y5_L in terms of external input signals:

$G2A = nG2A\_nL$

$G2B = nG2B\_nL$

$Y5 = nY5\_nL$

$Y5\_L = nY5 = n(G1 \;.\; nG2A\_nL \;.\; nG2B\_nL \;.\; C \;.\; nB \;.\; A)$

$= nG1 + G2A\_L + G2B\_L + nC + B + nA$

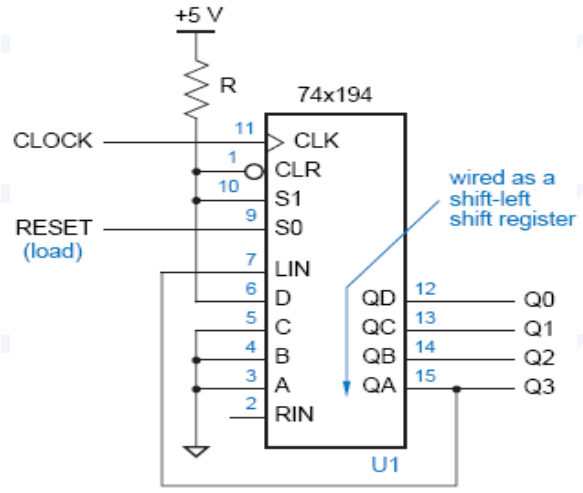
Table 5-7

74x138 – Truth Table

Inputs						Outputs							
G1	nG2a	nG2b	C	B	A	nY7	nY6	nY5	nY4	nY3	nY2	nY1	nY0
0	x	x	x	x	x	1	1	1	1	1	1	1	1
x	1	x	x	x	x	1	1	1	1	1	1	1	1
x	x	1	x	x	x	1	1	1	1	1	1	1	1
1	0	0	0	0	0	1	1	1	1	1	1	1	0
1	0	0	0	0	1	1	1	1	1	1	1	0	1
1	0	0	0	1	0	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	0	1	1	1
1	0	0	1	0	0	1	1	1	0	1	1	1	1
1	0	0	1	0	1	1	1	0	1	1	1	1	1
1	0	0	1	1	0	1	0	1	1	1	1	1	1
1	0	0	1	1	1	0	1	1	1	1	1	1	1

3. *4 bit Ring counter: schematic, explain its operation, main waveforms*

The simplest shift-register counter uses an n-bit shift register to obtain a counter with n states, and is called a ring counter. Figure shows the logic diagram for a 4-bit ring counter.

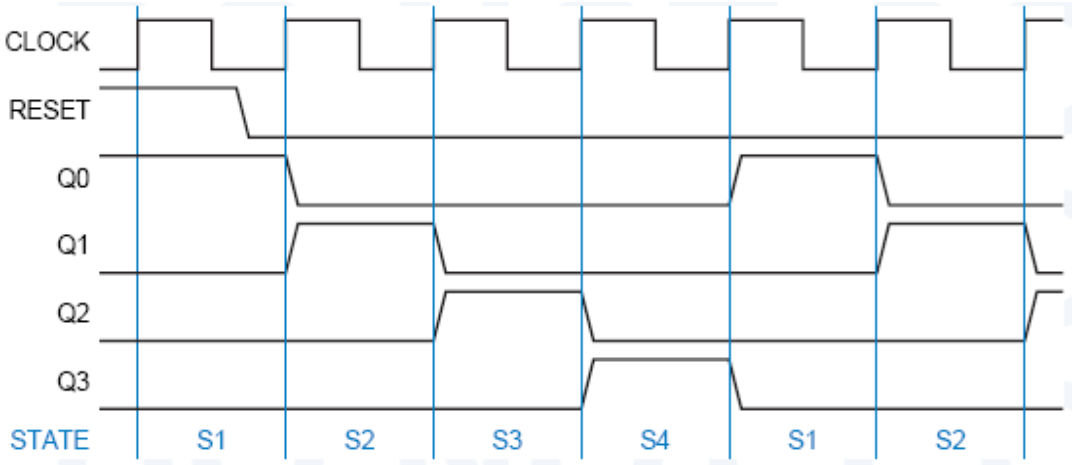


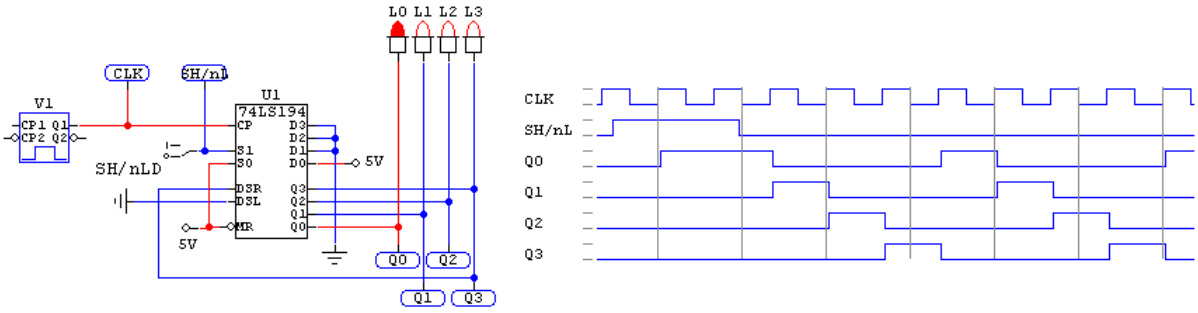
The 74x194 universal shift register is wired so that it normally performs a left shift. However, when RESET is asserted, it loads 0001 (refer to the '194's function table).

Once RESET is negated, the ’194 shifts left on each clock tick. The LIN serial input is connected to the “leftmost” output, so the next states are 0010, 0100, 1000, 0001, 0010, ….

Thus, the counter visits four unique states before repeating.

A timing diagram is shown. An n-bit ring counter visits n states in a cycle.





Ring counter with 74LS194 and timing diagrams

	CLK	Q_0	Q_1	Q_2	Q_3	**Explicaţie**
Initializare	0	0	0	0	0	nMR = 0
	1	1	0	0	0	S1 S0 = 11 (parallel load)
Complete cycle: 4 CLKs	2	0	1	0	0	S1 S0 = 01 (shift right)
	3	0	0	1	0	
	4	0	0	0	1	
	5 (1)	1	0	0	0	

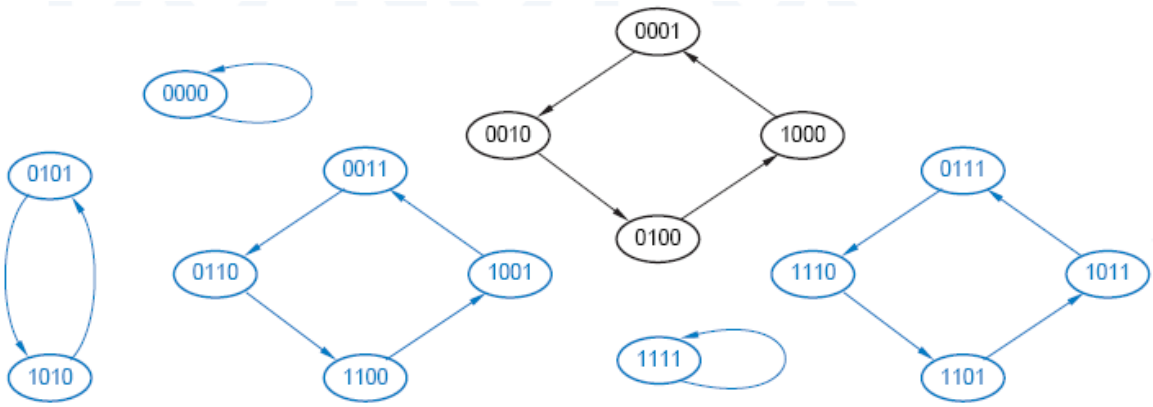
The ring counter already introduced has one major problem—it is not robust.

If its single 1 output is lost due to a temporary hardware problem (e.g., noise), the counter goes to state 0000 and stays there forever.

Likewise, if an extra 1 output is set (i.e., state 0101 is created), the counter will go through an incorrect cycle of states and stay in that cycle forever.

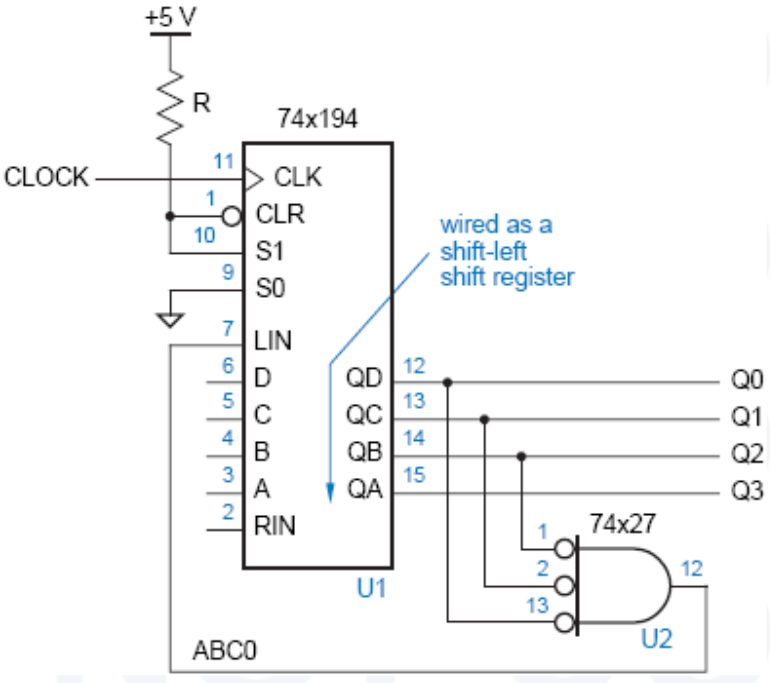
These problems are quite evident if we draw the complete state diagram for the counter circuit, which has 16 states.

As shown, there are 12 states that are not part of the normal counting cycle. If the counter somehow gets off the normal cycle, it stays off it.



4. *Self correcting counters built around registers. Give at least 2 examples: schematic, explain its operation, main waveforms*

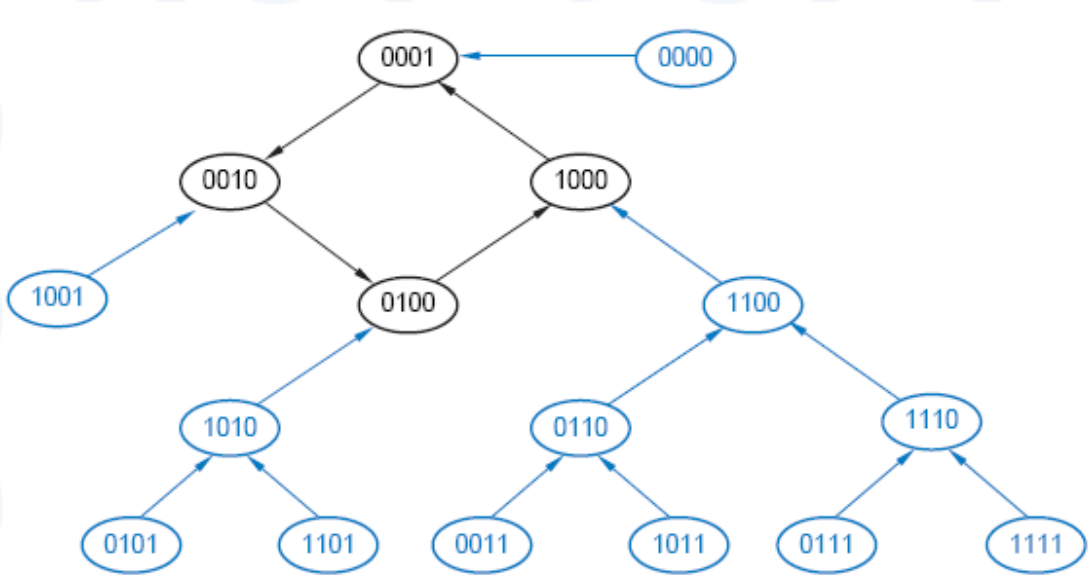
A self-correcting ring counter circuit is shown. The circuit uses a NOR gate to shift a 1 into LIN only when the three least significant bits are 0.



Notice that, in this circuit, an explicit RESET signal is not necessarily required. Regardless of the initial state of the shift register on power up, it reaches state 0001 within four clock ticks.

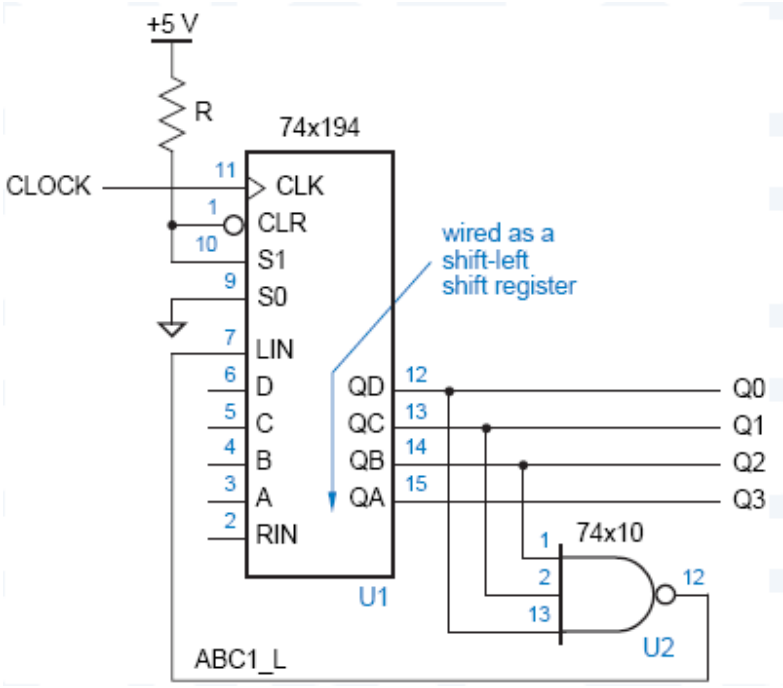
Therefore, an explicit reset signal is required only if it is necessary to ensure that the counter starts up synchronously with other devices in the system or to provide a known starting point in simulation.

This results in the state diagram; all abnormal states lead back into the normal cycle.



For the general case, an n-bit self-correcting ring counter uses an n-1-input NOR gate, and corrects an abnormal state within n - 1 clock ticks.

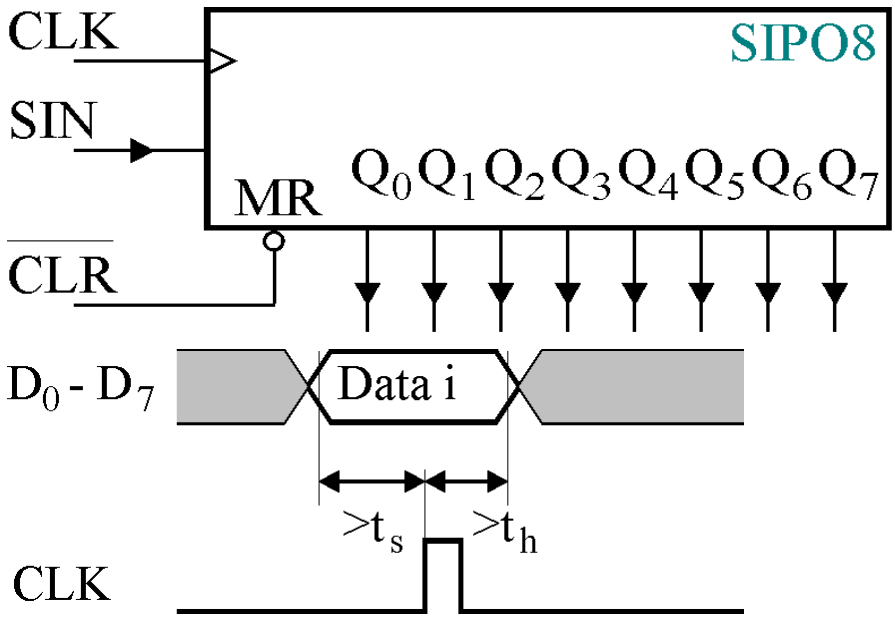
In CMOS and TTL logic families, wide NAND gates are generally easier to come by than NORs, so it may be more convenient to design a self-correcting ring counter as shown in figure. States in this counter's normal cycle have a single circulating 0.



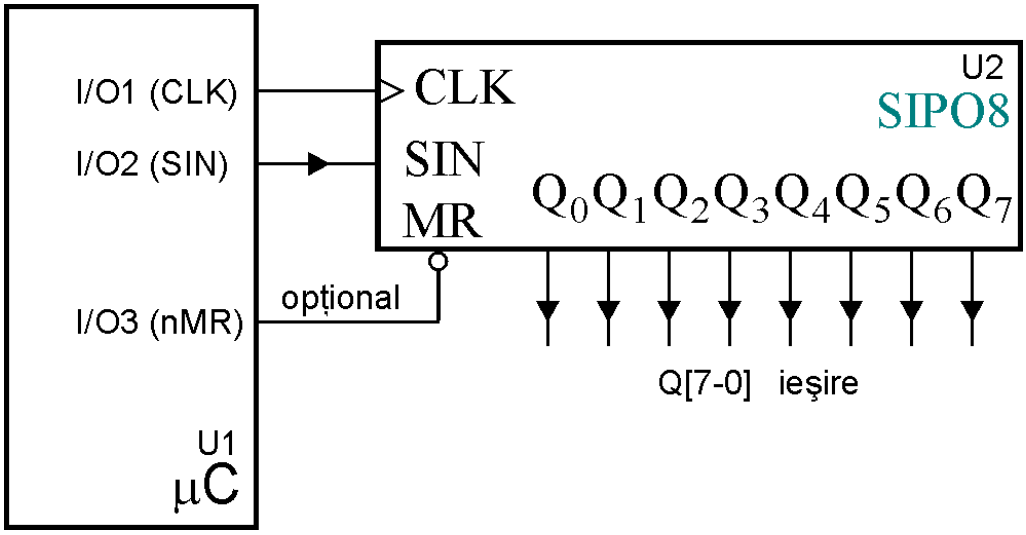
5. *Describe how to achieve parallel-to-serial, respectively serial-to-parallel data conversion*

Serial – parallel conversion

Uses a SIPO register:



Used for expanding the output pins for a low count pin microprocessor system
E.g. PIC16F84A has 18 pini, 13 are I/O
2 pins are used and extra 8 outputs are provided

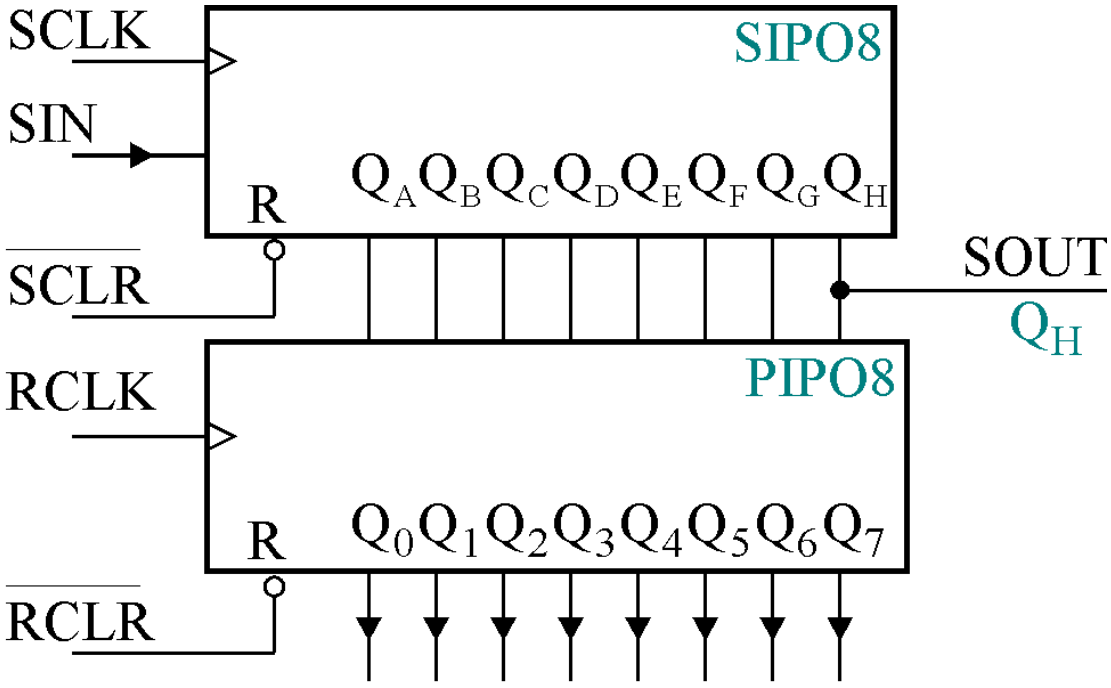


Expanding the output lines of a microcontroller

Serial – parallel conversion

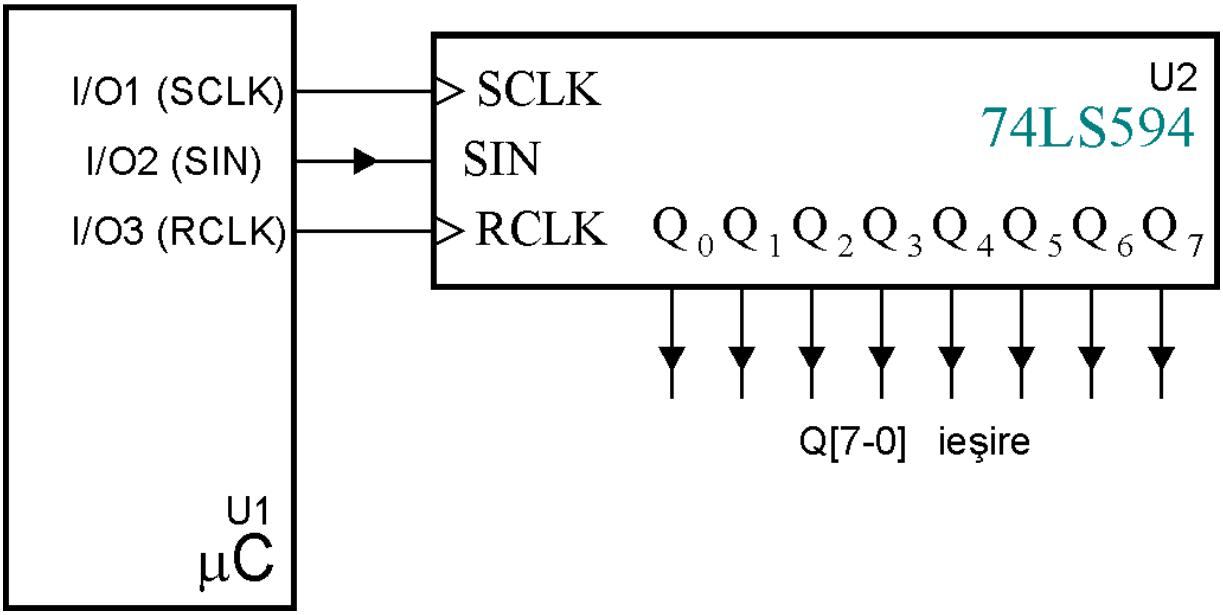
Problems when connecting fast devices

Solution: 74LS594 register



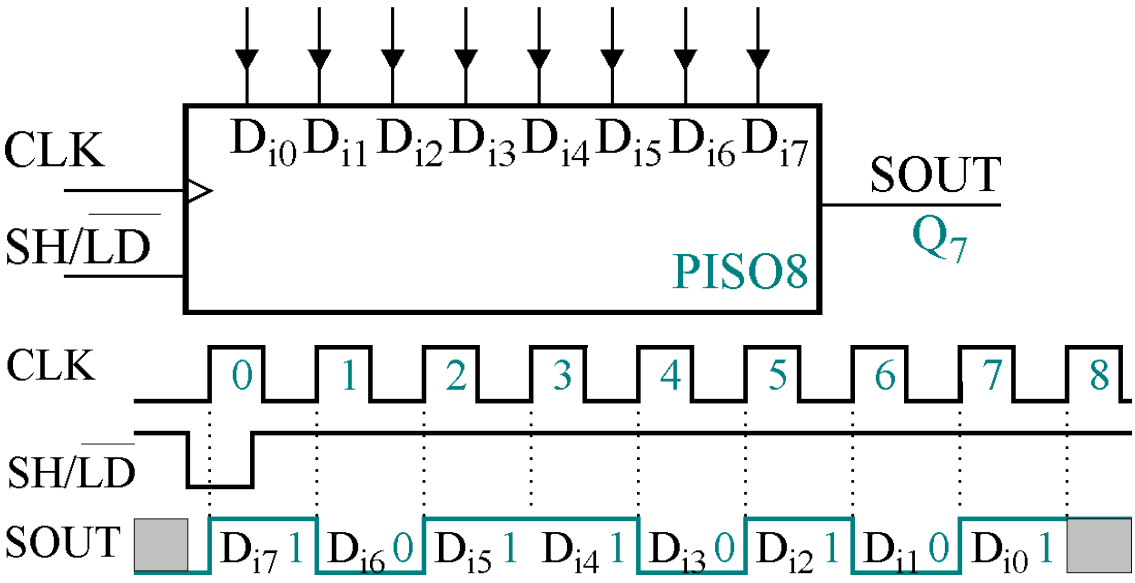
74LS594 – functional diagram

Serial – parallel conversion



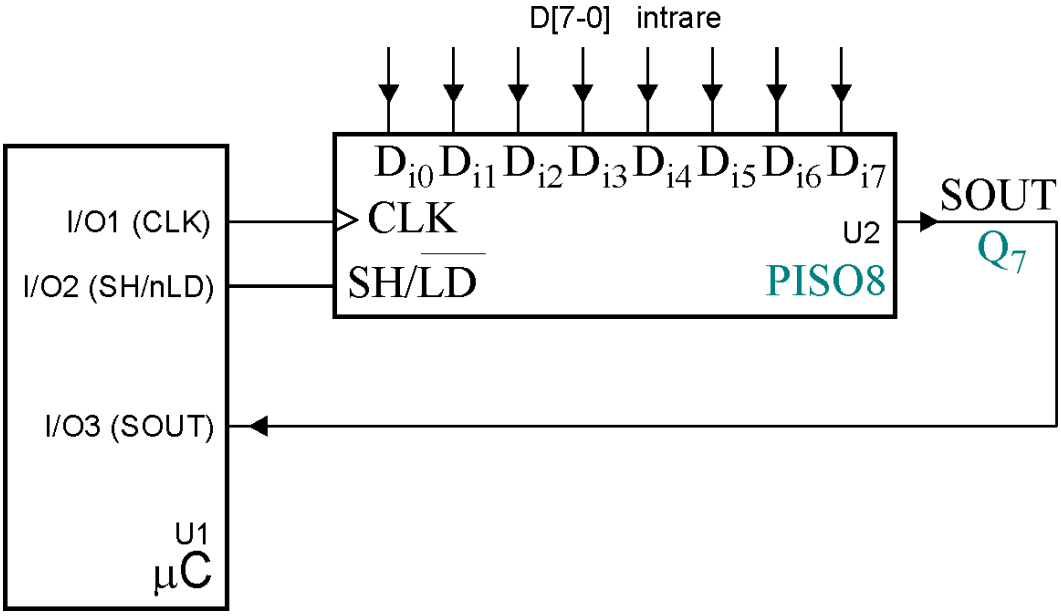
Expanding the Output lines of a microcontroller, 2nd version

Uses a PISO register:



Parallel – serial conversion

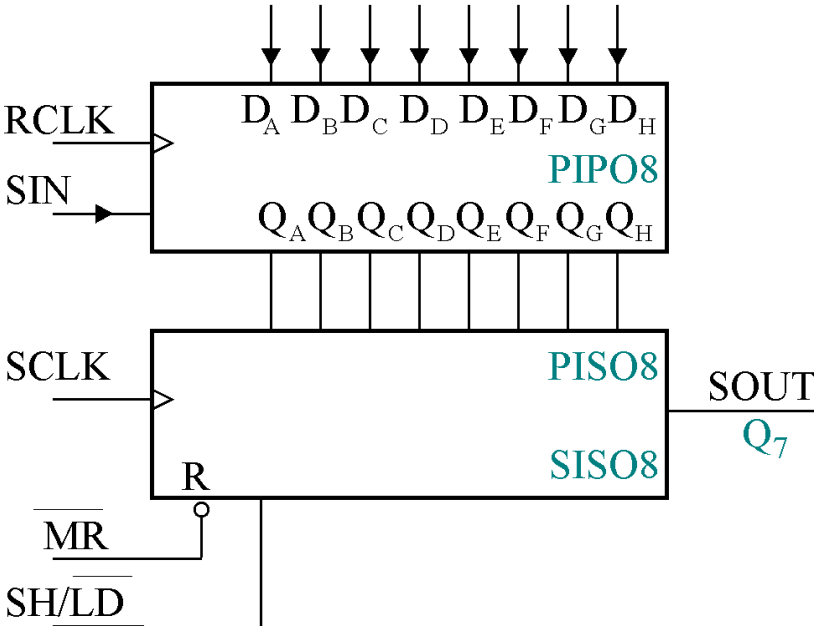
Parallel – serial conversion can be used to expand the input lines in a microcontroller system



Parallel – serial conversion

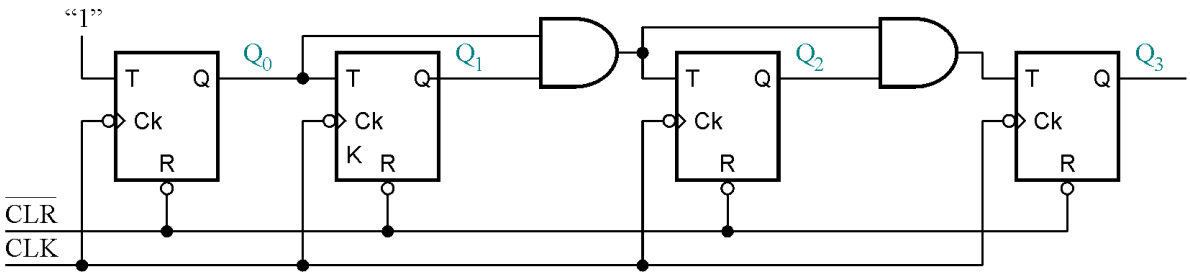
Same problem as before (with fast devices)

Solution: 74LS597 register



74LS597 – functional diagram

6. *4-bit binary synchronous counter. Draw the schematic diagram, explain its operation, and draw the relevant waveforms*

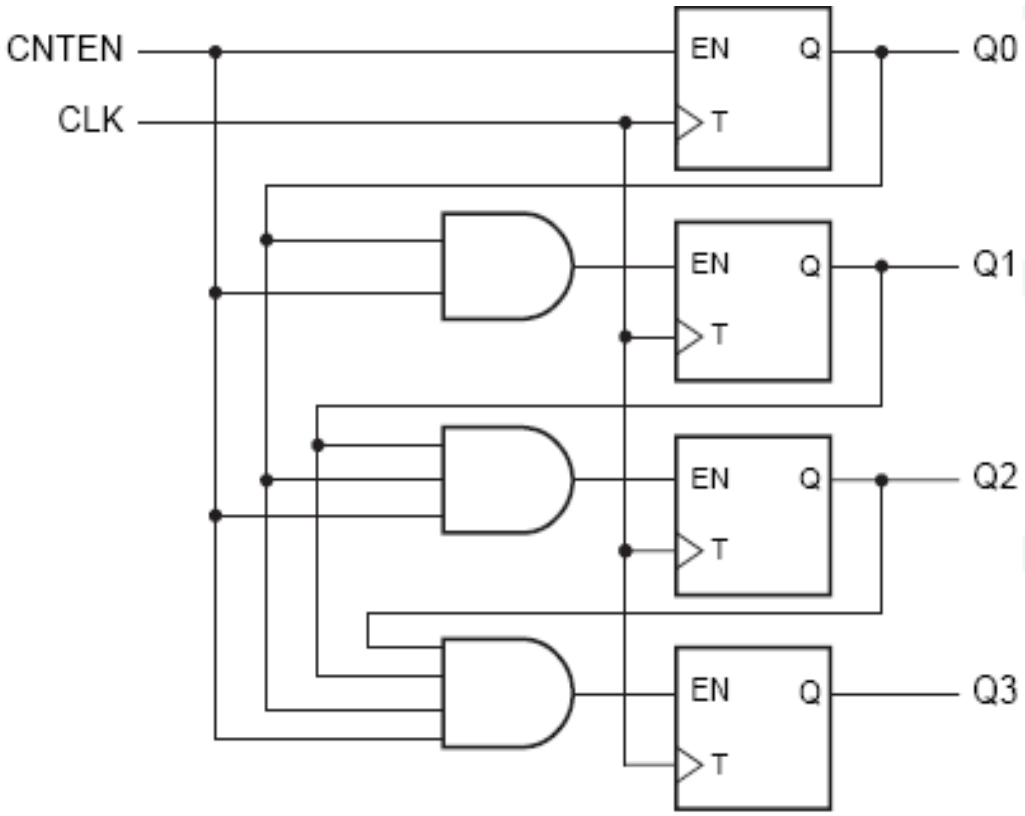


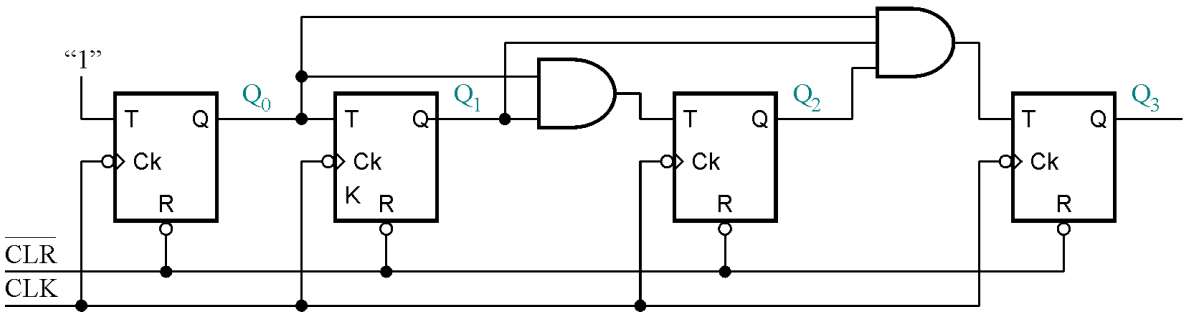
The counter structure previous presented is sometimes called a synchronous serial counter because the combinational enable signals propagate serially from the least significant to the most significant bits.

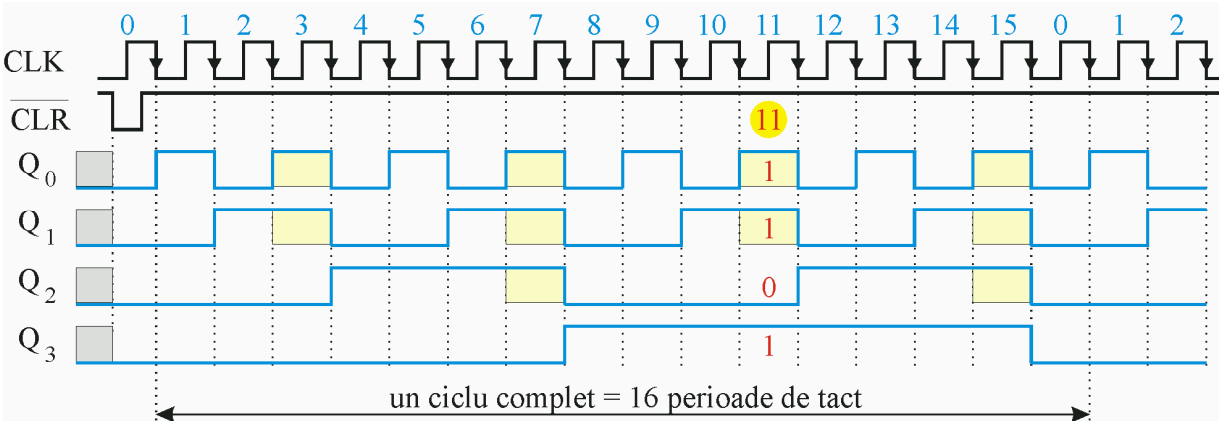
If the clock period is too short, there may not be enough time for a change in the counter's LSB to propagate to the MSB**.**

This problem is eliminated by driving each EN input with a dedicated AND gate, just a single level of logic.

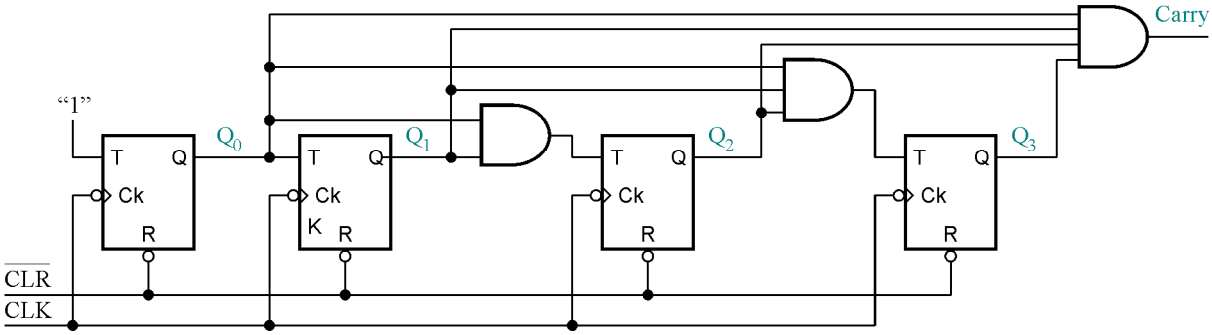
Called a synchronous parallel counter, this is the fastest binary counter structure**.**







Adding Output Carry Feature



7. *Outline the main methods for obtaining modulus p frequency dividers and programmable frequency dividers*

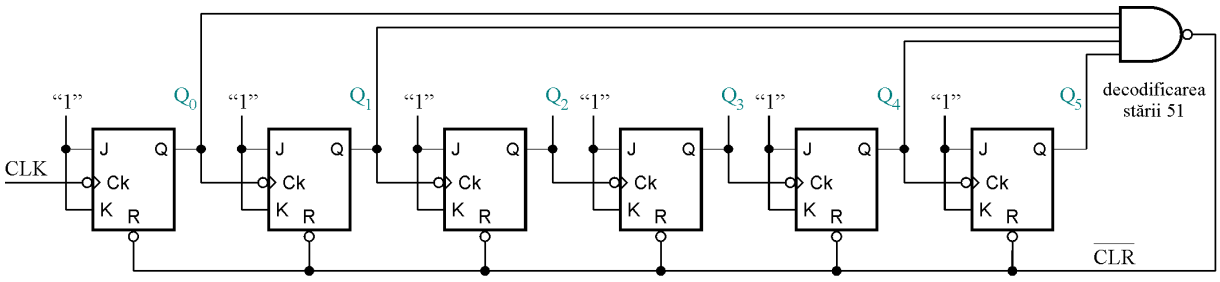
Modulus p Counter Design

Let p = 51

There are log251 = 6 flip flops needed

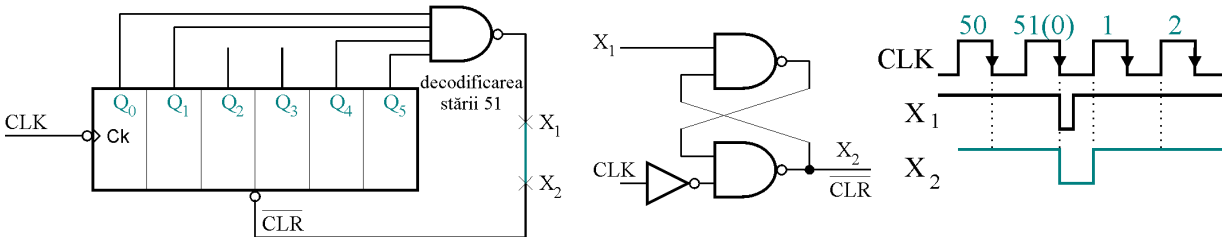
p = 51 = 1*32 + 1*16 + 0*8 + 0*4 +1*2 + 1*1

p = 1100112

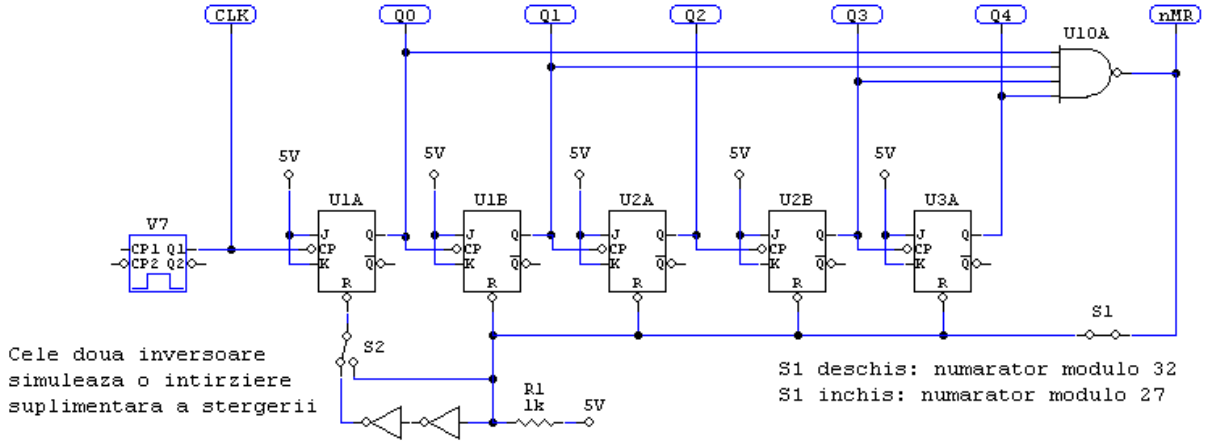


32	16	8	4	2	1
$Q_5 = 1$	$Q_4 = 1$	$Q_3 = 0$	$Q_2 = 0$	$Q_1 = 1$	$Q_0 = 1$

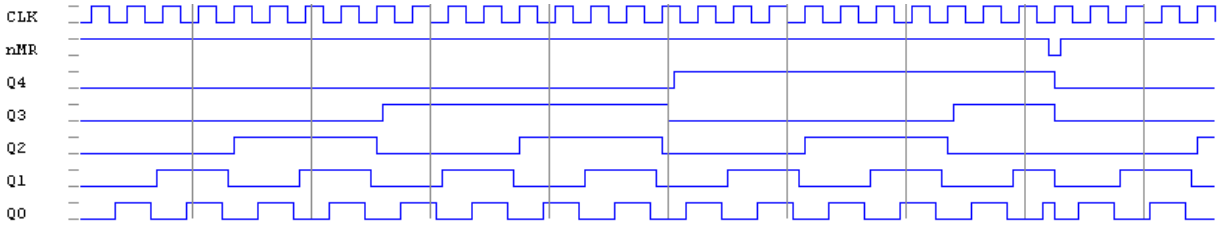
A latch to store the internal nCLR signal is needed



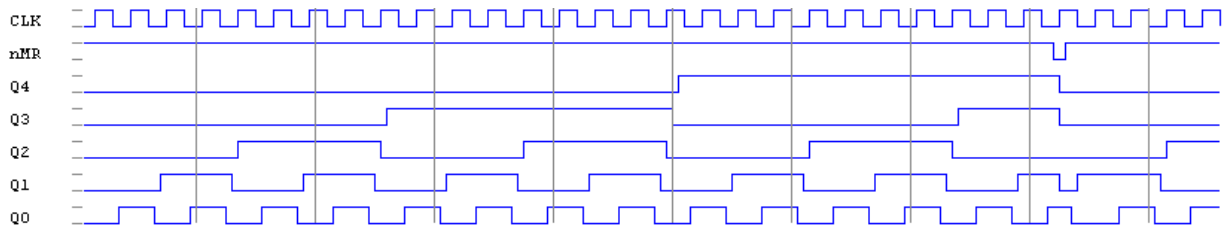
Simulation for p = 27



Ripple counter (p = 27) – simulated delayed Reset signal

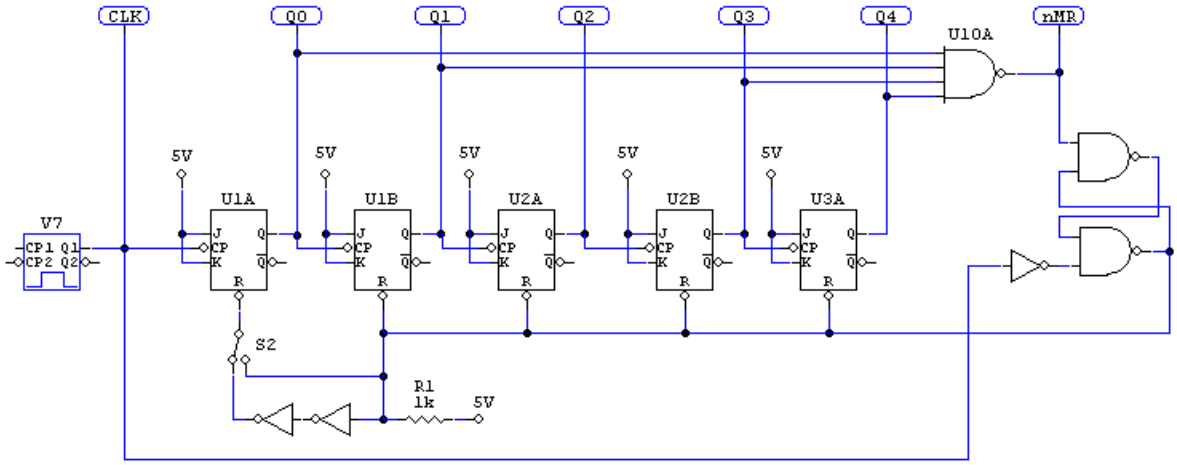


Modulus 27 counter, correct timing (S1 ON, S2 – to right)

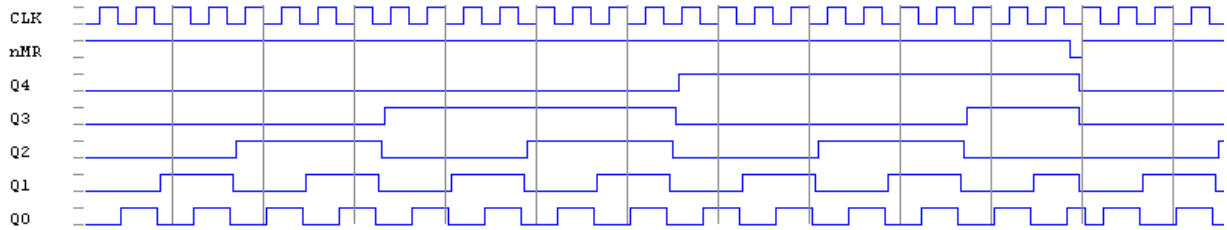


Modulus 27 counter, incorrect timing (S1 ON, S2 – to left) Sequence is ...26, 27+ CLR, 2, 3, ...

Adding the SR Latch



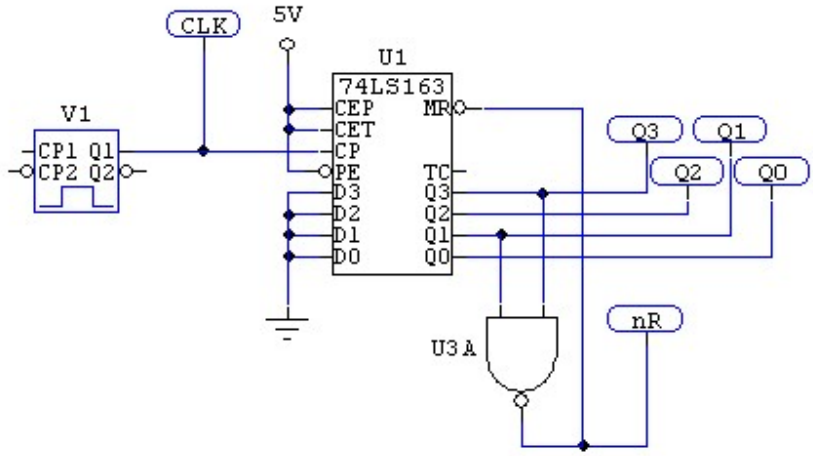
Correct timing



S1 ON, S2 to left

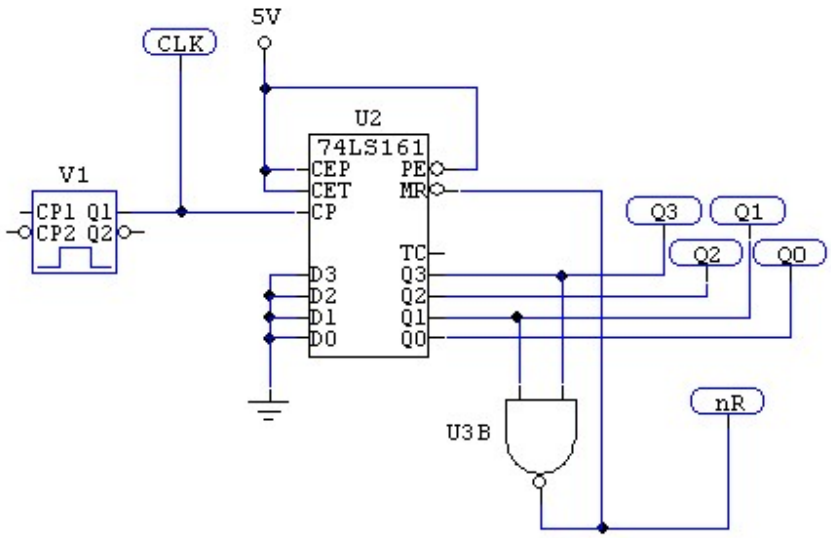
8. *Influence of Sync / Async Reset (explain using waveforms and a 74x163 based counter.*

Influence of Sync / Async Reset



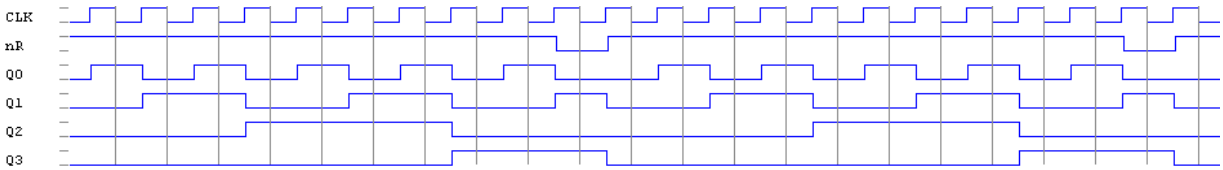
74x163 - Synchronous Reset

Modulus = 11

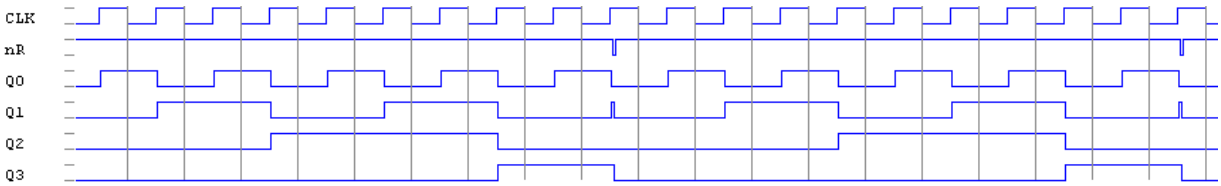


74x161 - Asynchronous Reset

Modulus = 10



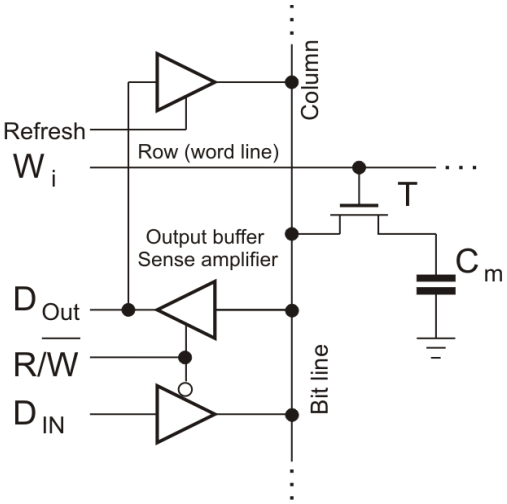
74x163 - Synchronous Reset – Modulus = 11



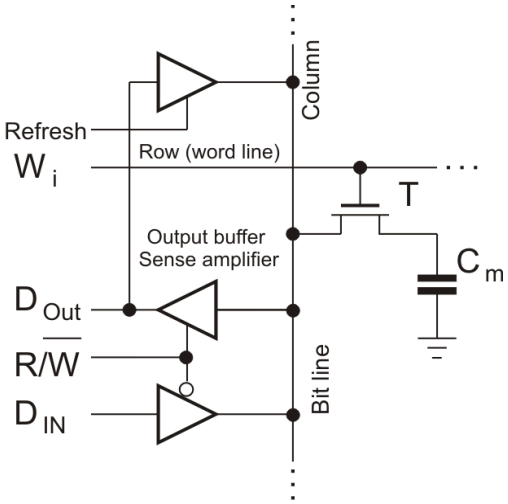
74x161 - Asynchronous Reset – Modulus = 10

9. *Explain briefly the operation of a DRAM - reading, writing, refresh*

DRAM – Write Operation

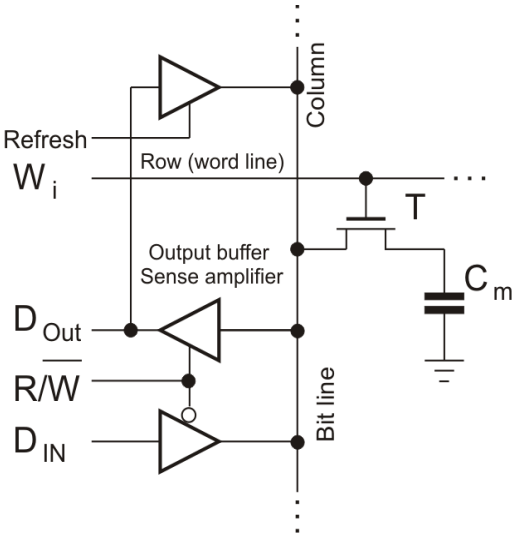


Writing a 1 into the memory cell

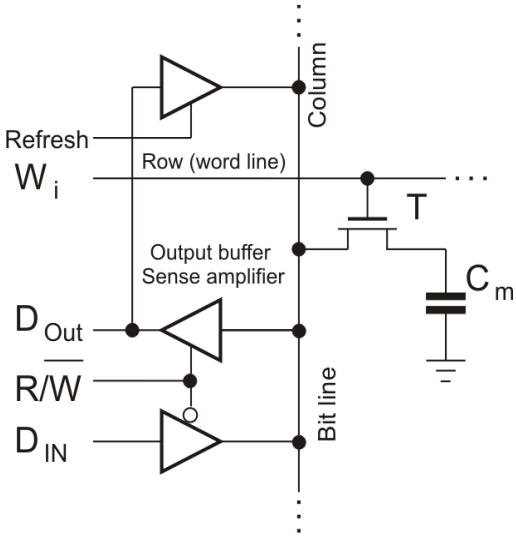


Writing a 0 into the memory cell

DRAM – Read Operation

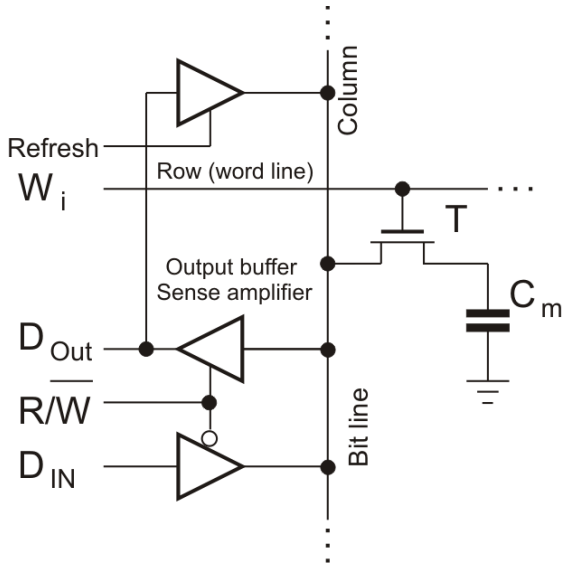


Reading a 1 from the memory cell

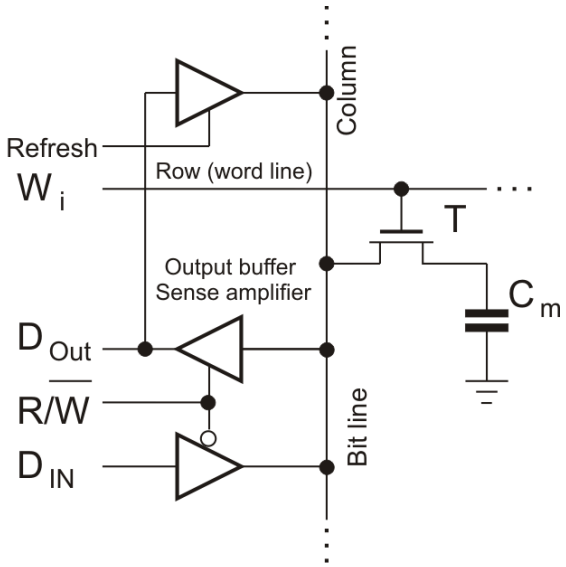


Reading a 0 from the memory cell

DRAM – Refresh Operation



Refreshing a stored 1



Refreshing a stored 0

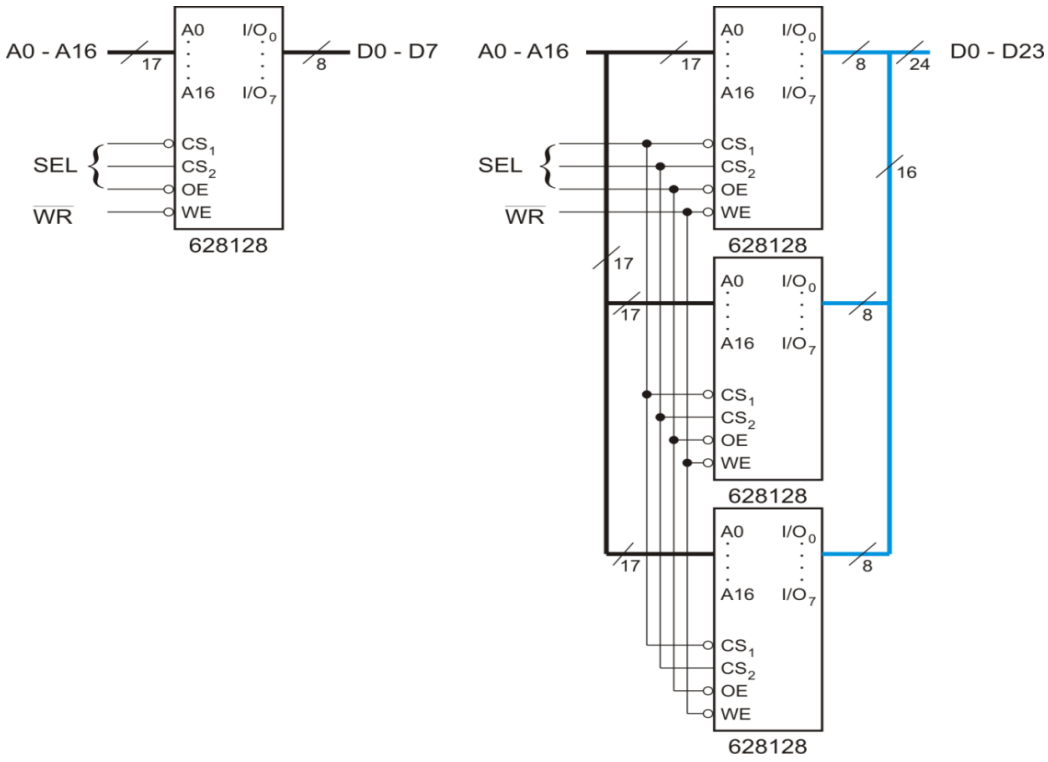
10. Memory extension techniques

Extending the Word Width

Word width extension 8 -> 24 bits

The initial memory

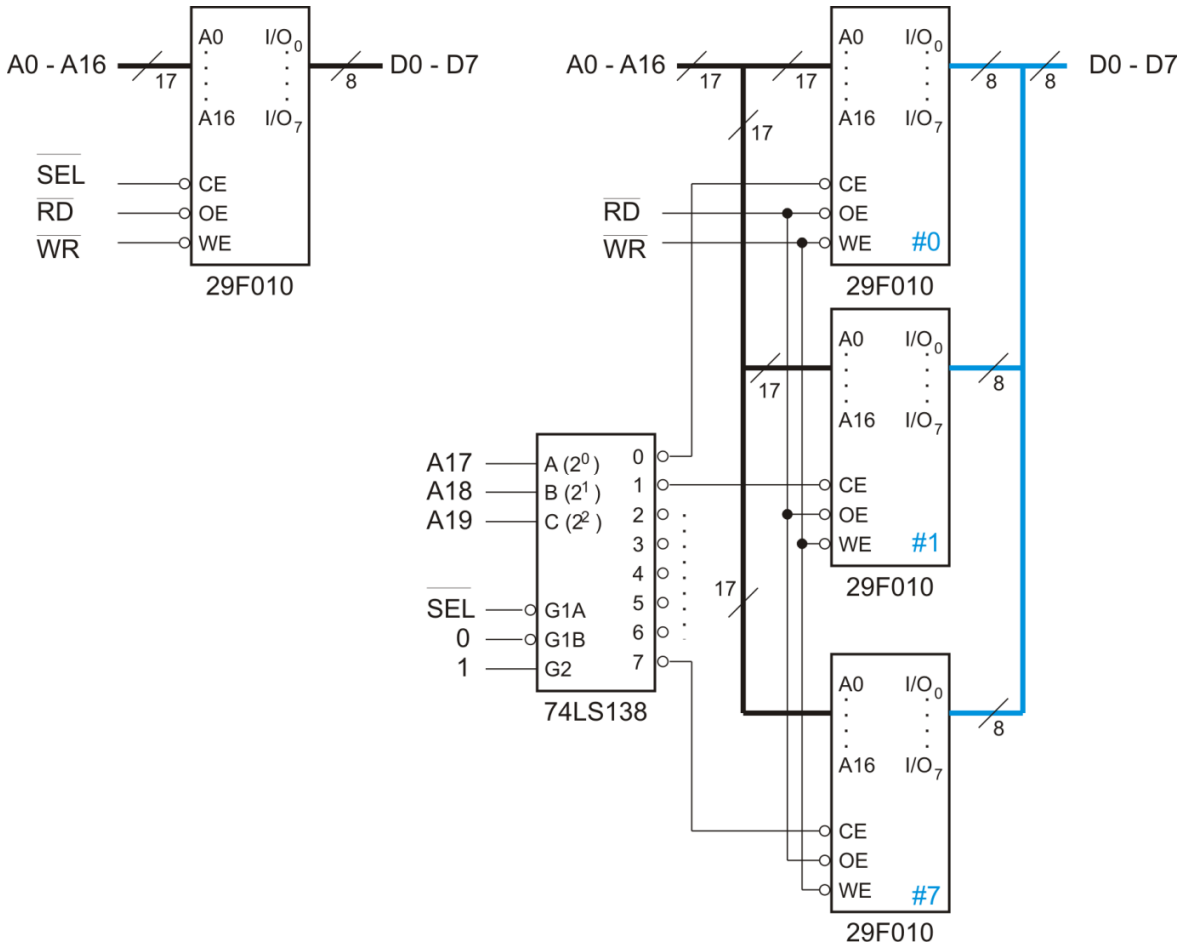
The extended memory



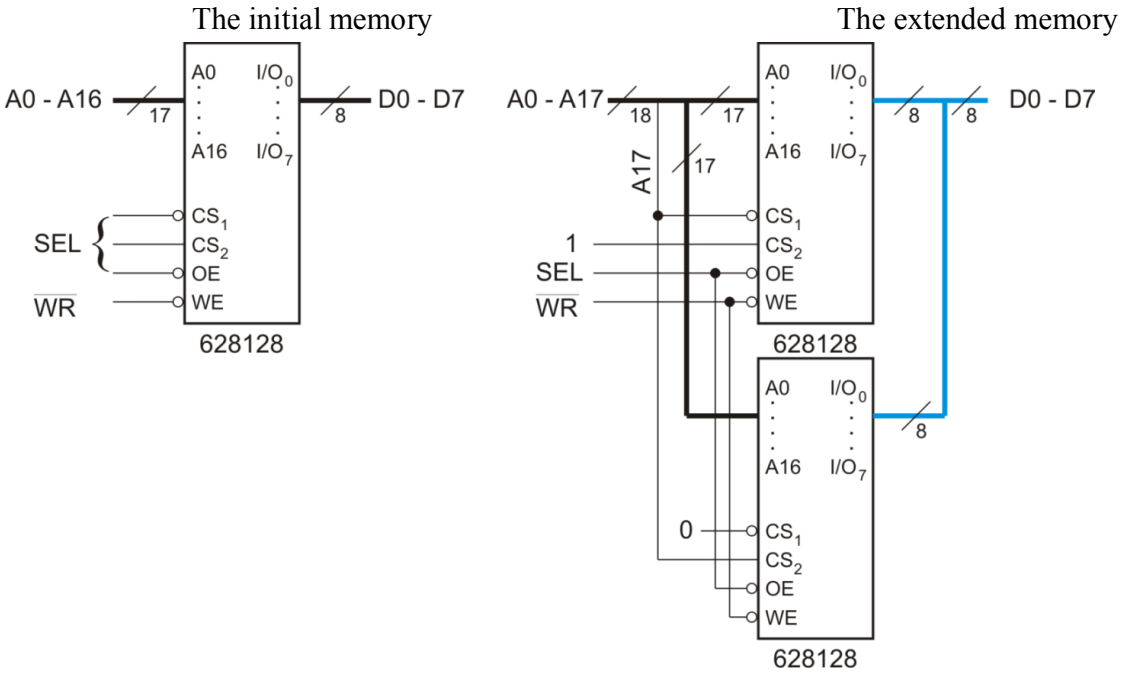
Extending the Number of Words

Extending the number of words (128 x 8 -> 1024 x 8 kbit)

The initial memory The extended memory

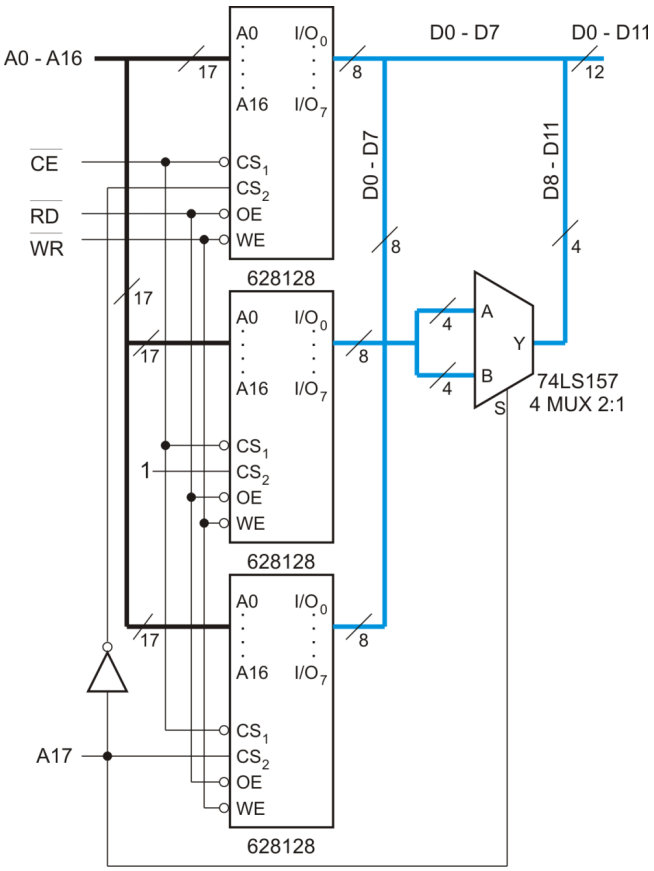

A0 - A16
17
A0
A16
I/O0
I/O7
8
D0 - D7
SEL
RD
WR
CE
OE
WE
29F010
A17
A18
A19
A (2^0)
B (2^1)
C (2^2)
G1A
G1B
G2
0
1
2
3
4
5
6
7
74LS138
#0
#1
#7

Doubling the capacity (128 to 256 kB)



Mixed Extension

Mixed extension: 128 k x 8 bit -> 256 k x 12 bit



Analog Integrated Circuits

1. *CC-CE, CC-CC and Darlington configurations – draw the schematics for these configurations and name the main parameters most often used to characterize these circuits. pg. 204, course #2*

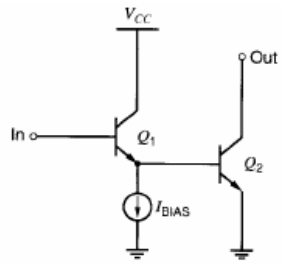


Fig. 1.

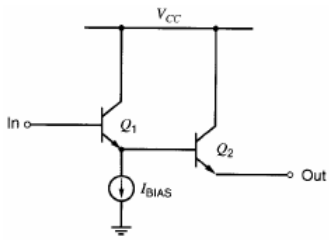


Fig. 2.

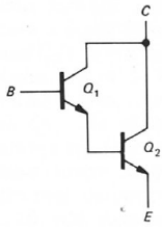


Fig. 3.

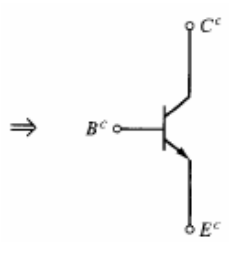


Fig.4.

(Abstract: These configuratios increase the input resistance and the current gain; the V_{BE} is twice the normal and the saturation voltage is at least V_{BE}.)

The common-collector - common-emitter (CC-CE), common-collector-common-collector (CC-CC), and Darlington configurations are all closely related. They incorporate an additional transistor to boost the current gain and input resistance of the basic bipolar transistor. The common-collector-common-emitter configuration is shown in Fig. 1. The biasing current source I_{BIAS} is present to establish the quiescent dc operating current in the emitter-follower transistor Ql**;** this current source may be absent in some cases or may be replaced by a resistor. The common-collector-common-collector configuration is illustrated in Fig. 2. In both of these configurations, the effect of transistor Q_l is to increase the current gain through the stage and to increase the input resistance.

The Darlington configuration, illustrated in Fig. 3, is a composite two-transistor device in which the collectors are tied together and the emitter of the first device drives the base of the second. A biasing element of some sort is used to control the emitter current of Ql**.** The result is a three-terminal composite transistor that can be used in place of a single transistor in common-emitter, common-base, and common-collector configurations. The term *Darlington* is often used to refer to both the CC-CE and CC-CC connections.

For the purpose of the low-frequency, small-signal analysis of circuits, the two transistors Q_l and Q_2 can be thought of as a single composite transistor, as illustrated in Fig. 4.

The composite transistor has much higher input resistance and current gain than a single transistor.

r_π^c is the resistance seen looking into the composite base BC with the composite emitter EC grounded (Fig 5):

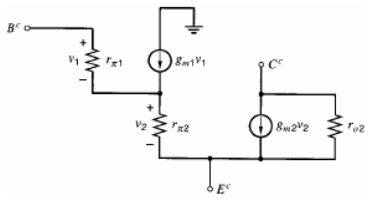


Fig. 5.

$$r_\pi^c = r_{\pi 1} + (\beta_0 + 1) r_{\pi 2}$$

For the special case in which the biasing current source I_{BIAS} is zero, the effective current gain β^c is the ratio:

$$\beta^c = \frac{i_c^c}{i_b^c} = \frac{i_{c2}}{i_{b1}}; = \frac{\beta_0 i_{b2}}{i_{b1}} = \frac{\beta_0 i_{e1}}{i_{b1}} = \frac{\beta_0(\beta_0+1) i_{b1}}{i_{b1}} = \beta_0(\beta_0+1)$$

The base-emitter drop is twice normal; the saturation voltage is at least one diode drop. The combination tends to act like a slow transistor; this is taken care of by including a resistor, R (few hundres Ohms – power transistor or a few thousend Ohms – small-signal Darlington).

2. *The bipolar cascode configuration – draw the circuit, compare its output resistance with that of the common emitter stage. pg. 207, course #2*

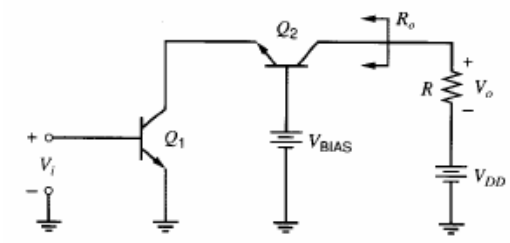


Fig. 6

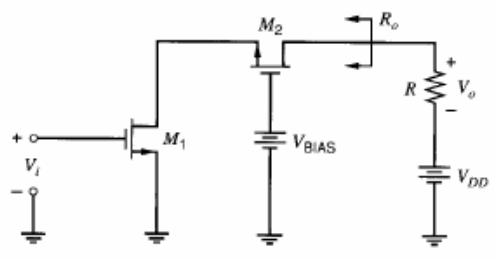


Fig. 7.

(Abstract: The cascode connection displays an output resistance that is larger by a factor of about β_0 than the CE stage alone.)

The cascode configuration is important mostly because it increases output resistance and reduces unwanted capacitive feedback in amplifiers, allowing operation at higher frequencies than would otherwise be possible. The high output resistance attainable is particularly useful in desensitizing bias references from variations in power-supply voltage and in achieving large amounts of voltage gain.

In bipolar form, the cascode is a common-emitter-common-base (CE-CB) amplifier, as shown in Fig. 6. The MOS version is shown in Fig. 7.The small-signal equivalent for the bipolar cascode circuit is shown in Fig. 8. The output resistance can be calculated by shorting the input v_i to ground and applying a test signal at the output. Then $v_1 = 0$ and the g_{mv1} generator is inactive (Fig. 9).

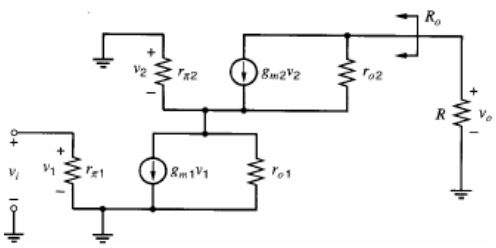


Fig. 8.

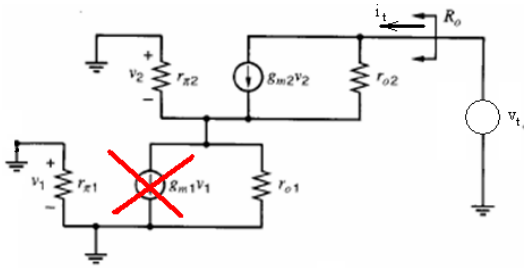


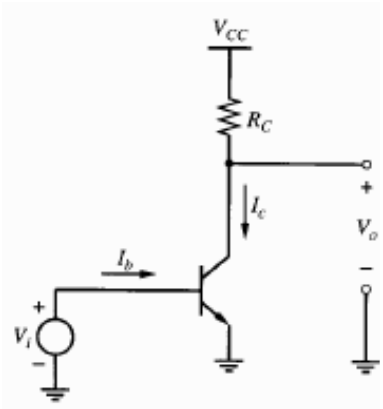
Fig. 9.

$$v_2 = -i_t\left(r_{\pi 2}\|r_{o1}\right) \qquad i_2 = i_t - g_{m2}v_2 = i_t\left[1 + g_{m2}\left(r_{\pi 2}\|r_{o1}\right)\right] \qquad v_t = -v_2 + i_2 \cdot r_{o2}$$

$$\Rightarrow R_o = \frac{v_t}{i_t} = r_{\pi 2}\|r_{o1} + r_{o2} + r_{o2}g_{m2}\cdot\left(r_{\pi 2}\|r_{o1}\right) \cong$$

$$\cong r_{o2}\left[1 + g_{m2}\cdot\left(r_{\pi 2}\|r_{o1}\right)\right] = r_{o2}\left[1 + g_{m2}\cdot\left(\frac{r_{\pi 2}r_{o1}}{r_{\pi 2} + r_{o1}}\right)\right] = r_{o2}\left(1 + \frac{g_{m2}r_{o1}}{1 + \frac{g_{m2}r_{o1}}{\beta_0}}\right)$$

If $g_{m2}r_{o1} >> \beta_0$ and $\beta_0 >> 1$ than $R_o \cong \beta_0 r_{o2}$



The cascode connection displays an output resistance that is larger by a factor of about β_0 than the CE stage alone (shown in Fig. 10) (we assumed that R_C is very large and can be neglected).

Fig. 10.

3. The dc transfer characteristic of an emitter-coupled pair - compare the schemes with and without emitter degeneration. We know the values for collector currents:

$$I_{c1} = \frac{\alpha_F I_{TAIL}}{1+\exp\left(-\frac{V_{id}}{V_T}\right)}; \qquad I_{c2} = \frac{\alpha_F I_{TAIL}}{1+\exp\left(\frac{V_{id}}{V_T}\right)}$$

pg. 215 – 217(abstract), course#2.

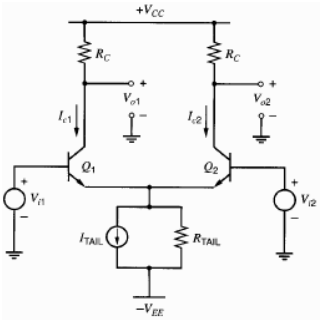


Fig. 11.

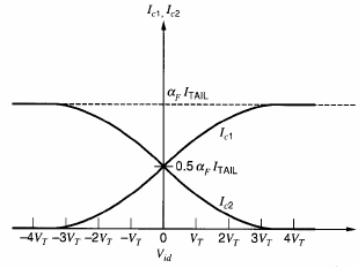


Fig. 12.

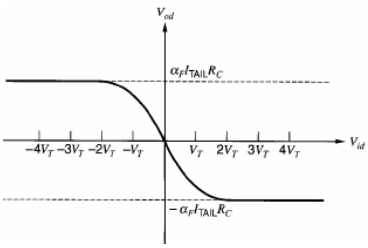


Fig. 13.

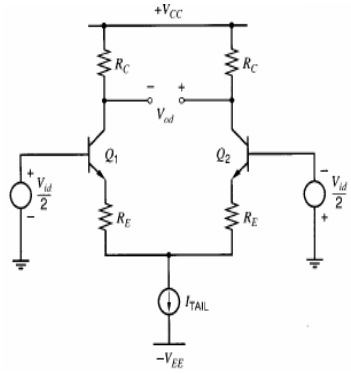


Fig. 14.

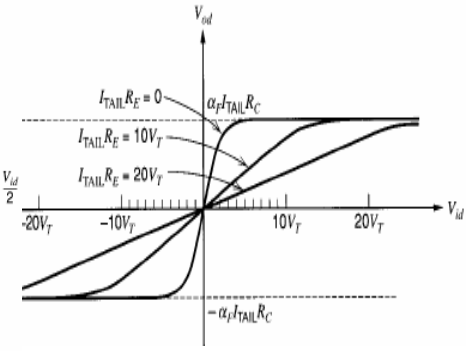


Fig. 15.

(Abstract: The circuit behaves in an linear fashion only when the magnitude of v_{id} is less than about V_T. The property „for v_{id}=0 we have v_{od}=0" allows direct coupling of cascaded stages. To increase the range of v_{id} emitter-degeneration resistors are included.)

The simplest form of an emitter-coupled pair is shown in Fig. 11. The large-signal behavior of the emitter-coupled pair is important in part because it illustrates the limited range of input voltages over which the circuit behaves almost linearly. These two currents are shown as a function of V_{id} in Fig. 12. When the magnitude of V_{id} is greater than about $3V_T$, the collector currents are almost independent of V_{id} because one of the transistors turns off and the other conducts all the current that flows. Furthermore, the circuit behaves in an approximately linear fashion only when the magnitude of V_{id} is less than about V_T . We can now compute the output voltages as:

$$V_{o1} = V_{cc} - I_{c1}R_C; \qquad V_{o2} = V_{cc} - I_{c2}R_C$$

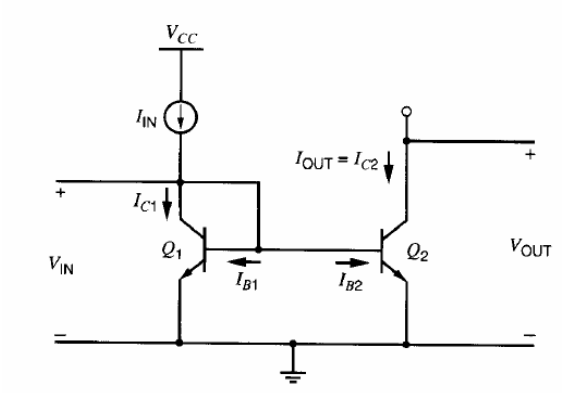
The output signal of interest is often the difference between V_{o1} and V_{o2}, which we define as V_{od}. Then:

$$V_{od} = V_{o1} - V_{o2} = \alpha_F I_{TAIL} R_C \tanh\left(\frac{-V_{id}}{2V_T}\right)$$

This function is plotted in Fig. 13. Here a significant advantage of differential amplifiers is apparent: when V_{id} is zero, V_{od} is zero if Q_1 and Q_2 are identical and if identical resistors are connected to the collectors of Q_1 and Q_2. This property allows direct coupling of cascaded stages without offsets.

To increase the range of V_{id} over which the emitter-coupled pair behaves approximately as a linear amplifier, emitter-degeneration resistors are frequently included, as shown in Fig.14. The effect of the resistors may be understood intuitively from the examples plotted in Fig. 15. For large values of emitter-degeneration resistors, the linear range of operation is extended by an amount approximately equal to I_{TAIL} R_E. Furthermore, since the voltage gain is the slope of the transfer characteristic, the voltage gain is reduced by approximately the same factor that the input range is increased.

4. *Simple current mirror - bipolar version. Draw the schematic and compare it with an ideal current mirror. pg. 256, course #4*



(Abstract : The output current for a simple current mirror must exactly mirror the input current but, in a real circuit, I_{OUT} is less then the input current, I_{IN}. Ideally**:** the output current is equal to the input current, independent of V_{OUT}, with $V_{IN} = 0$. A current mirror must provide a constant current at the output and an infinity output resistance.)

Fig. 16.

Ideally: the output current is equal to the input current multiplied by a desired current gain (if the gain is unity - **current mirror**); the current-mirrors gain is independent of input frequency; the output current is independent of the voltage between the output and common terminals; the voltage between the input and common terminals is ideally zero because this condition allows the entire supply voltage to appear across the input current source; more than one input and/or output terminals are sometimes used.

The simplest form of a current mirror consists of two transistors. Fig. 16 shows a bipolar version of this mirror. Transistor Q1 is diode connected, forcing its collector-base voltage to zero. In this mode, Q_1 operates in the forward-active region. Assume that Q_2 also operates in the forward-active region and that both transistors have infinite output resistance. Then I_{OUT} is controlled by $V_{BE2} = V_{BE1}$ (KVL).

$$V_{BE2} = V_T \ln\frac{I_{C2}}{I_{S2}} = V_{BE1} = V_T \ln\frac{I_{C1}}{I_{S1}}$$

$$\Rightarrow I_{C2} = \frac{I_{S2}}{I_{S1}} I_{C1} \quad \text{and if} \quad I_{S1} = I_{S2} \quad \text{shows that} \quad I_{C1} = I_{C2}$$

$$I_{IN} - I_{C1} - \frac{I_{C1}}{\beta_F} - \frac{I_{C2}}{\beta_F} = 0 \qquad I_{OUT} = I_{C2} = I_{C1} = \frac{I_{IN}}{1 + \frac{2}{\beta_F}}$$

$$\Rightarrow I_{C2} = \frac{I_{S2}}{I_{S1}} I_{C1} = \left(\frac{I_{S2}}{I_{S1}} I_{IN}\right)\left(\frac{1}{1 + \frac{1 + (I_{S2}/I_{S1})}{\beta_F}}\right)$$

In practice, the devices need not be identical.

At the input:

$$V_{IN} = V_{CE1} = V_{BE1} = V_{BE(on)}$$

Since $V_{BE(on)}$ is proportional to the natural logarithm of the collector current, V_{IN} changes little with changes in bias current.

The minimum output voltage required to keep Q_2 in the forward-active region is:

$$V_{OUT(min)} = V_{CE2(sat)}$$

5. Wilson current mirror – draw the schematic of the bipolar version, estimate the value of the output resistance and compare it with that of the cascode current mirror pg. 277, Course#6

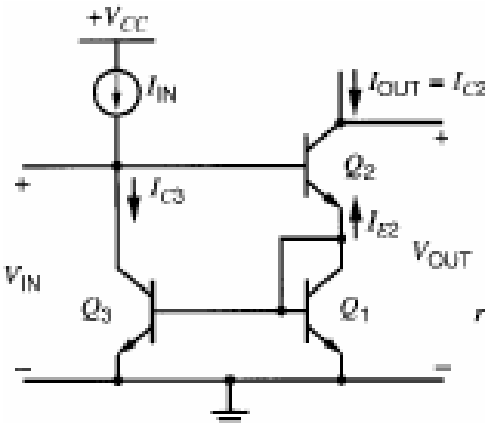


Fig. 17.

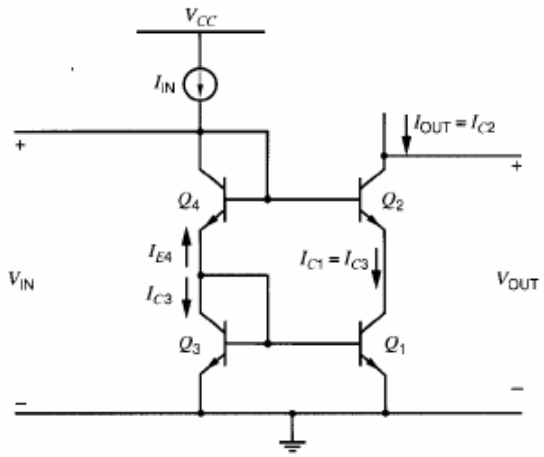


Fig. 18.

(Abstract: Both circuits, the Wilson current mirror and the cascode current mirror achieve a very high output resistance: $R_o \approx \frac{\beta_0 r_{o2}}{2}$)

The Wilson current mirror is shown in Fig. 17, the cascode current mirror is shown in Fig. 18. Both circuits, the Wilson current mirror and the cascode current mirror achieve a very high output resistance. A small - signal analysis shows that R_o, with some approximations, has the value:

$$R_o \approx \frac{\beta_0 r_{o2}}{2}$$

In the cascode current mirror, the small-signal current that flows in the base of Q2 is mirrored through Q3 to Ql so that the small-signal base and emitter currents leaving Q2 are approximately equal.

On the other hand, in the Wilson current mirror, the small-signal current that flows in the emitter of Q2 is mirrored through Q1 to Q3 and then flows in the base of Q2. Although the cause and effect relationship here is opposite of that in a cascode current mirror, the output resistance is unchanged because the small-signal base and emitter currents leaving Q2 are still forced to be equal. Therefore, the small-signal collector current of Q2 that flows because of changes in the output voltage still splits into two equal parts with half flowing in $r_{\pi 2}$.

6. Bipolar Widlar Current Source - draw the schematic, explain why it is not a current mirror. pg. 300, course#8

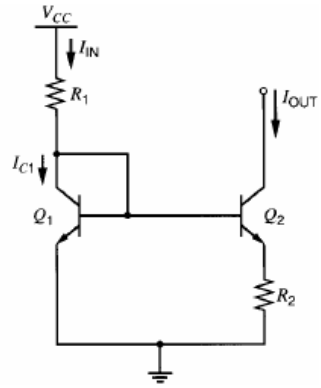


Fig. 19.

(Abstract: In the Widlar current source the transistors Q_1 and Q_2 operate with unequal base emitter voltages. This circuit is referred to as a current source rather than a current mirror because the output current, I_{OUT}, is much smaller than the input current, I_{IN}.)

In the Widlar current source of Fig. 19, the resistor R_2 is inserted in series with the emitter of Q_2, and transistors Q_1 and Q_2 operate with unequal base emitter voltages if $R_2 \neq 0$. This circuit is referred to as a current source rather than a current mirror because the output current is much less dependent on the input current and the power-supply voltage than in the simple current mirror.

Assume that Q_1 and Q_2 operate in the forward active region. KVL around the base-emitter loop gives:

$$V_{BE1} - V_{BE2} - \frac{\beta_F + 1}{\beta_F} I_{OUT} R_2 = 0 \qquad \Rightarrow V_T \ln \frac{I_{C1}}{I_{S1}} - V_T \ln \frac{I_{OUT}}{I_{S2}} - \frac{\beta_F + 1}{\beta_F} I_{OUT} R_2 = 0$$

$$\text{If} \quad \beta \to \infty \quad \text{and} \quad I_{s1} = I_{s1} \qquad \Rightarrow V_T \ln \frac{I_{IN}}{I_{OUT}} = I_{OUT} R_2$$

This transcendental equation can be solved by trial and error to find I_{OUT} if R_2 and I_{IN} are known, as in typical analysis problems. Because the logarithm function compresses changes in its argument, attention can be focused on the linear term, I_{OUT} R_2, simplifying convergence of the trial-and-error process. In design problems, however, the desired I_{IN} and I_{OUT} are usually known, and the equations provides the required value of R_2.

The Widlar source allows currents in the microamp range to be realized with moderate values of resistance. It is possible to write the final equation like this:

$$I_{IN} = I_{OUT} e^{\frac{I_{OUT} R_2}{V_T}}$$

It is obvious that I_{OUT} is much smaller than I_{IN}.

Exemple: I_{IN} = 1 mA, R2= 5 KΩ, I_{OUT} = 20 μA

7. Temperature-Insensitive Bias with band gap voltage reference: the motive, the idea, one of the practical implementations. Pg. 317, course #9

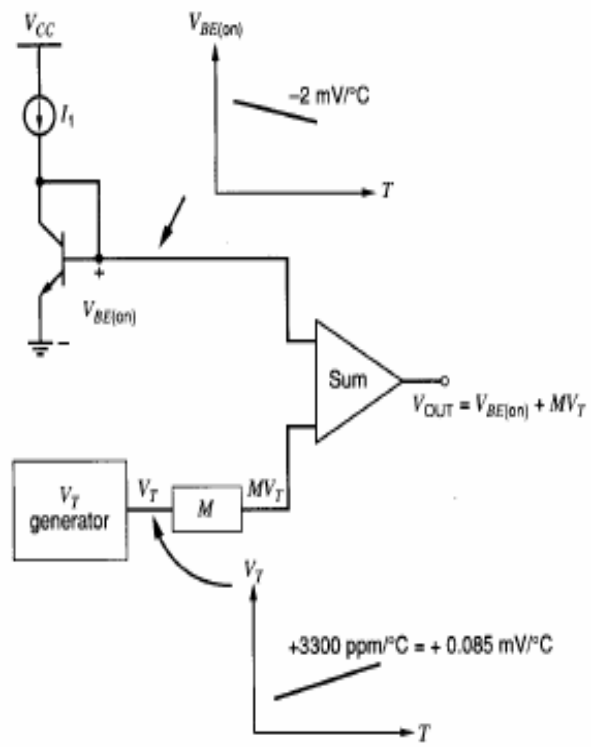


Fig. 20.

(Abstract: We need low-temperature-coefficient reference voltages. The idea is shown in Fig. 20. – 2mV/°C temperature-coefficient of V_{BE} to be compensated with a component with +2mV/°C coefficient temperature.)

In practice, requirements often arise for low-temperature-coefficient voltage bias or reference voltages. The voltage reference for a voltage regulator is a good example.

Since $V_{BE(on)}$ and V_T have opposite T_{CF}, the possibility exists for referencing the output current to a composite voltage that is a weighted sum of $V_{BE(on)}$ and V_T. By proper weighting, zero temperature coefficient should be attainable. So we can obtain low-temperature-coefficient voltage bias or reference voltages.

$$V_{OUT} = V_{BE(on)} + MV_T$$

The idea is shown in Fig. 20. – 2mV/°C temperature-coefficient of V_{BE} to be compensated with a component with +2mV/°C coefficient temperature. One possibility is to use V_T which T_{CF} is about +0,085 mV/°C.

A bandgap voltage reference is a voltage reference circuit widely used in integrated circuits usually with an output voltage around 1.25 V, close to the theoretical band gap of silicon at 0°K. A practical implementation is shown in Fig. 21.

$$V_{RC1} = V_{RC2} \Rightarrow I_{C1} = I_{C2}$$

$$V_{R1} = I_{C1}R_1 = V_{BE2} - V_{BE1} =$$

$$= V_T \ln\frac{I_{C2}}{I_S} - V_T \ln\frac{I_{C1}}{I_S} = V_T \ln\frac{I_{C2}}{I_{C1}} = V_T \ln n$$

$$V_{R2} = R_2(I_{C1} + I_{C2}) = R_2\left(\frac{V_T \ln n}{R_1} + n\frac{V_T \ln n}{R_1}\right) =$$

$$= \frac{R_2}{R_1}(n+1)V_T \ln n = N \cdot V_T$$

$$\frac{dV_{R2}}{dT} = N\frac{dV_T}{dT} = N\frac{k}{q} = N\frac{kT}{qT} = N\frac{V_T}{T} = +2\frac{mV}{^\circ C}$$

$$\Rightarrow N = 2\cdot 10^{-3}\,\frac{300}{26\cdot 10^{-3}} \cong 23$$

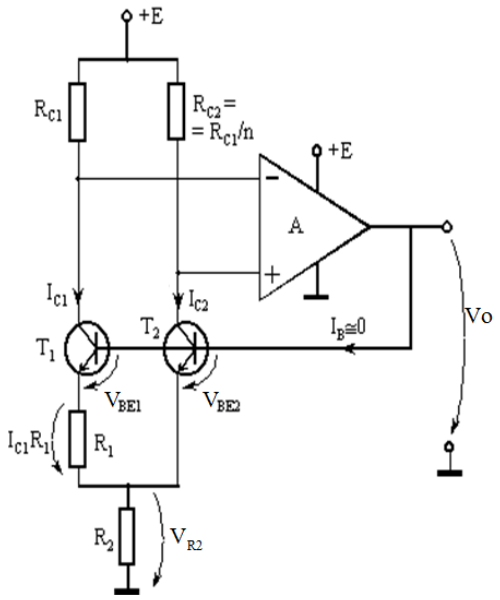


Fig. 21.

8. *Inverting and noninverting amplifier built with an ideal op amp - draw the schematics and find the gains, define the characteristics of an ideal op amp. pg. 406, 408, course #9*

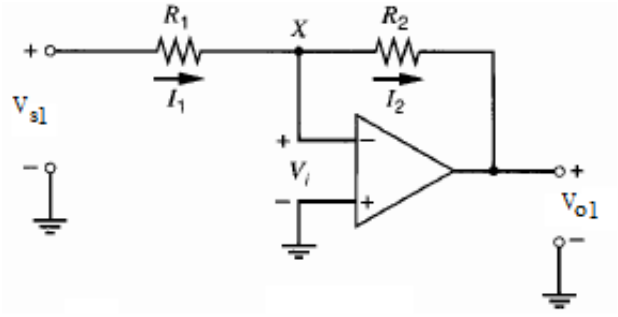


Fig. 22.

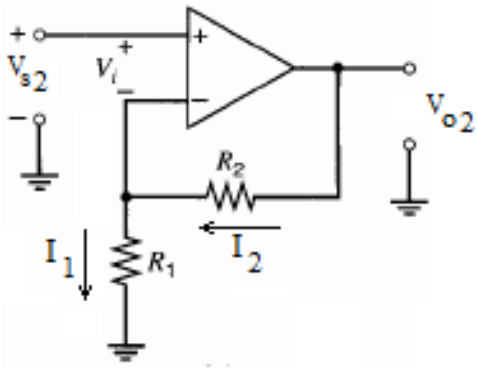


Fig. 23.

(Abstract: The golden rules: 1.The output attempts to do whatever is necessary to make the voltage difference between the inputs zero (in Fig. 22 and Fig. 23, $V_i = 0$). 2.The inputs draw no current)

An ideal op amp with a single-ended output has a differential input, infinite voltage open-loop gain, infinite input resistance, and zero output resistance. While actual op amps do not have these ideal characteristics, their performance is usually sufficiently good that the circuit behavior closely approximates that of an ideal op amp in most applications. These characteristics lead to the golden rules for op-amps. They allow us to logically deduce the operation of any op-amp circuit.

Fig. 22 shows an inverting amplifier build with an op amp. Considering we have an ideal op amp. First, because no current enters in the ”-” input, at the nod X we can write:

$$I_1 = I_2 \qquad (1)$$

Second, $V_i = 0$ and at the inverting input we have a ” virtual ground”. Then the voltage V_{s1} is across R_1 and Vo1 is across R_2. In the first equation we can replace I_1 and I_2 with the values:

$$I_1 = \frac{V_{s1}}{R_1} \qquad I_2 = \frac{-V_{o1}}{R_2}$$

Equation (1) becames:

$$\frac{V_{s1}}{R_1} = -\frac{V_{o1}}{R_2} \Leftrightarrow V_{o1} = -V_{s1}\frac{R_2}{R_1}$$

This is the relationship between the output voltage and the input voltage for an inverting amplifier build with an op amp. A similar calculation can be done for the noninverting amplifier build with an ideal op amp (Fig. 23). The same, for Fig. 23:

$$I_1 = I_2 \qquad (2)$$

But we don’t have a virtual ground anymore: at the noninverting input is V_{s2}. In this case we can write:

$$I_1 = \frac{V_{s2}}{R_1} \qquad I_2 = \frac{V_{o2} - V_{s2}}{R_2}$$

Using this values in (2) we get the relationship between the output voltage and the input voltage for a noninverting amplifier build with an op amp:

$$\frac{V_{s2}}{R_1} = \frac{V_{o2} - V_{s2}}{R_2} \Leftrightarrow V_{o2} = \left(1 + \frac{R_2}{R_1}\right)V_{s2}$$

9. *Integrator, differentiator build with op amp - draw the schematics, find the relationships between input and output voltages. pg. 410, Course #10*

The integrator (Fig. 24) and the differentiator circuits (shown in Fig. 25) are examples of using op amps with reactive elements in the feedback network to realize a desired frequency response or time-domain response.

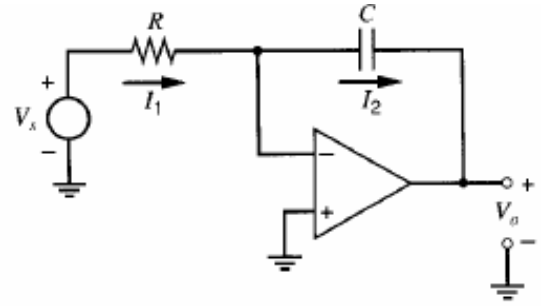


Fig. 24.

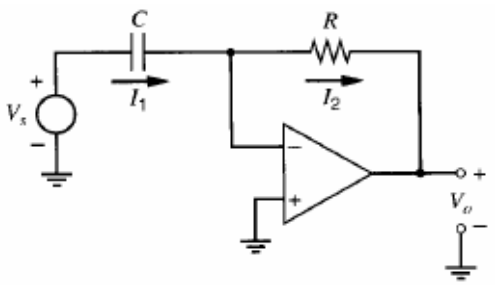


Fig. 25.

(Abstract: In the case of the integrator the output voltage is proportional to the integral of the input voltage with respect to time. In the case of the differentiator the output voltage is proportional to the time rate of change of the input voltage.)

In the case of the integrator (Fig. 24), the resistor R is used to develop a current I_1 that is proportional to the input voltage, V_s. This current flows into the capacitor C, whose voltage is proportional to the integral of the current I_2 with respect to time. Since the output voltage is equal to the negative of the capacitor voltage, the output is proportional to the integral of the input voltage with respect to time. In terms of equations:

$$I_1 = \frac{V_s}{R} = I_2 \qquad V_o = -\frac{1}{C}\int_0^t I_2 d\tau + V_o(0) \quad \Rightarrow V_o(t) = -\frac{1}{RC}\int_0^t V_s(\tau)d\tau + V_o(0)$$

In the case of the differentiator (Fig. 25), the capacitor C is connected between V_s and the inverting op-amp input. The current through the capacitor is proportional to the time derivative of the voltage across it (V_c), which is equal to the input voltage ($V_c = V_s$). This current flows through the feedback resistor R, producing a voltage at the output proportional to the capacitor current, which is proportional to the time rate of change of the input voltage. In terms of equations:

$$I_1 = C\frac{dV_s}{dt} = I_2 \qquad V_o = -RI_2 = -RC\frac{dV_s}{dt}$$

10. Improved precision half-wave rectifier - draw the schematic, the equivalent ones, the diadrames and explain the operation. pg.705, Course #10

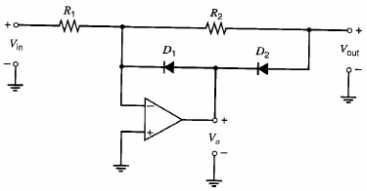


Fig. 26.

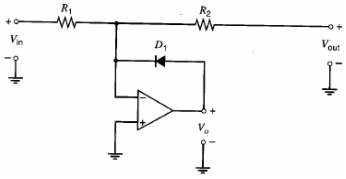


Fig. 27.

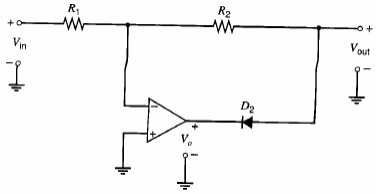
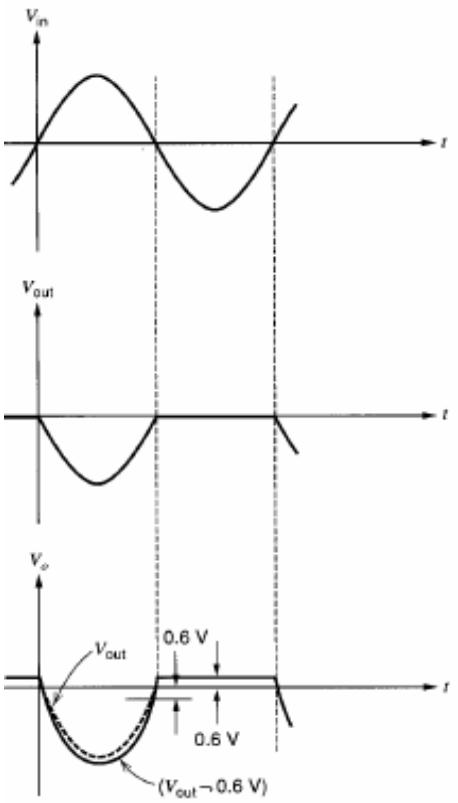


Fig. 28.



(Abstract: The schematic for an improved precision half-wave rectifier is shown in Fig. 26. Fig. 27 shows the equivalent circuit for $V_i<0$ and Fig. 28 shows the equivalent circuit for $V_i>0$. Fig. 29 shows the waveforms within the improved precision rectifier for a sinusoidal input, V_{in}; the output of the circuit is V_{out} and V_o is the op amp's output.)

Fig. 29

For input voltages less than zero, the equivalent circuit is shown in Fig. 27. Diode D_1 is forward biased and the op amp is in the active region. The inverting input of the op amp is clamped at ground by the feedback through D_1, and, since no current flows in R_2, the output voltage is also at ground. When the input voltage is made positive, no current can flow in the reverse direction through D_1 so the output voltage of the op amp V_o is driven in the negative direction. This reverse biases D_1 and forward biases D_2. The resulting equivalent circuit is shown in Fig. 28 and is simply an inverting amplifier with a forward-biased diode in series with the output lead of the op amp. Because of the large gain of the op amp, this diode has no effect on its behavior as long as it is forward biased, and so the circuit behaves as an inverting amplifier giving an output voltage of:

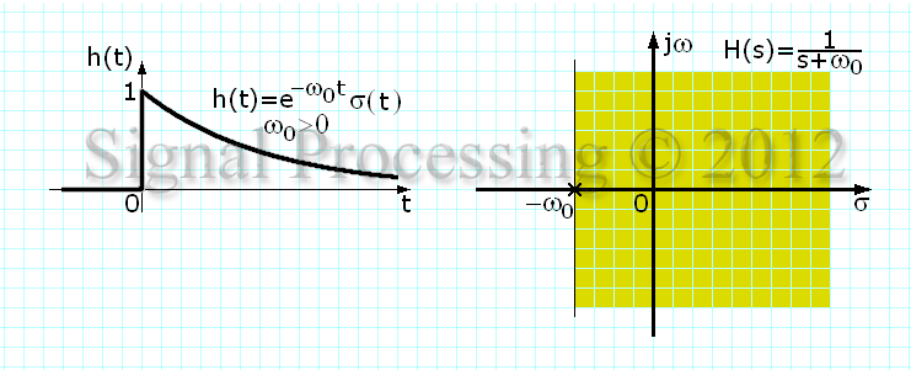
$$V_{out} = -\frac{R_2}{R_1} V_{in}$$

As shown in Fig. 29, the output voltage of the operational amplifier need only change in value by approximately two diode drops when the input signal changes from positive to negative.

Signal Processing

1. *Where are the poles of a stable and causal analog system? Give an example.*

The poles of a stable and causal system are located in the left half plane LHP while its zeros can be located anywhere in the complex plane. Example: $h(t)=\exp(-\omega_0 t)\sigma(t), \omega_0>0$. The transfer function is $H(\omega)=\frac{1}{s+\omega_0}$ with one pole, $s_p=-\omega_0$.



2. *Define minimum phase analog systems. Give an example.*

Systems having poles and zeros placed in the left half plane are named minimum phase systems. Consider the system with the impulse response

$h(t)=e^{-t}\sigma(t)\leftrightarrow H_u(s)=\frac{1}{s+1}$. It has one pole in the LHP and no zeros; hence it is a minimum phase system:

$H(\omega)=\frac{1}{1+j\omega}$, with $|H(\omega)|=1/\sqrt{1+\omega^2}, \Phi(\omega)=-arctg\omega$.

as opposed to another system with the frequency response:

$$H_{\omega_0}(\omega)=\frac{1}{1+j\omega}\frac{1-j\frac{\omega}{\omega_0}}{1+j\frac{\omega}{\omega_0}}\longleftrightarrow h_{\omega_0}(t)=\frac{1}{\omega_0-1}\left[(\omega_0+1)e^{-t}-2\omega_0 e^{-\omega_0 t}\right]\sigma(t)$$

with $\Phi_{\omega_0}(\omega)=-arctg\omega-2arctg\frac{\omega}{\omega_0}=\Phi(\omega)-2arctg\frac{\omega}{\omega_0}$.

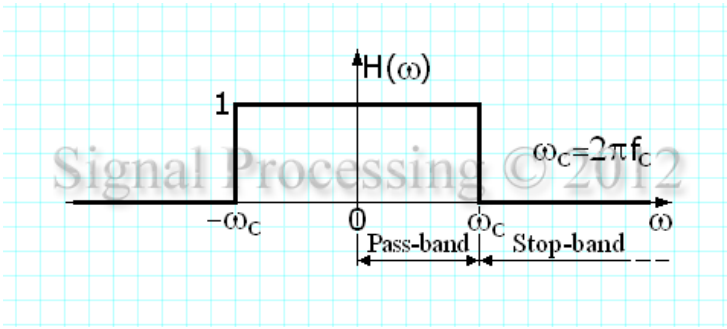
Both systems have the same amplitude-frequency characteristic but the second system introduces extra phase versus the first system.

3. *Ideal low pass filter. Frequency response and impulse response.*

The ideal low pass filter has the frequency response:

$$H(\omega) = p_{\omega_c}(\omega) \leftrightarrow h(t) = \frac{\sin \omega_c t}{\pi t}$$

It does not fulfill Paley-Wiener theorem.



4. *Enunciate WKS sampling theorem.*

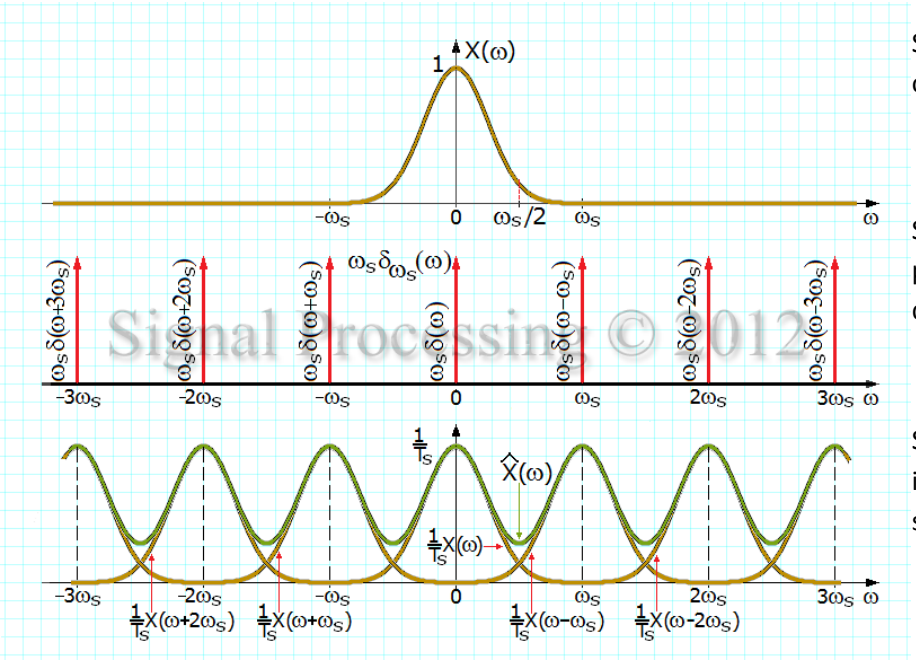
If the finite energy signal $x(t)$ is band limited at ω_M , ($X(\omega)=0$ for $|\omega| > \omega_M$), it is uniquely determined by its samples $\{x(nT_s) | n \in \square\}$ if the sampling frequency is higher or equal than twice the maximum frequency of the signal:

$$\omega_s \geq 2\omega_M$$

5. *Spectrum of ideal sampled signal (Relation + Graphical representation).*

$$\hat{x}(t) = \sum_{k=-\infty}^{\infty} x(kT_s)\delta(t - kT_s) \leftrightarrow \hat{X}(\omega) = \frac{1}{T_S} \sum_{k=-\infty}^{\infty} X\left(\omega - k\frac{2\pi}{T_S}\right)$$

The spectrum of an ideal sampled signal is the periodic repetition of the spectrum of the original signal. The period is inverse proportional with the sampling step T_S.

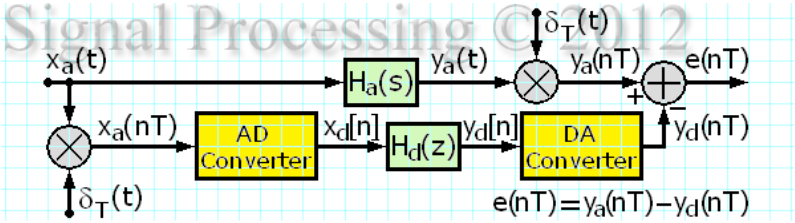


Spectrum of original signal

Spectrum of periodic Dirac distribution

Spectrum of ideal sampled signal

6. *Approximation of continuous-time systems with discrete-time systems using impulse invariance method.*



The system (not necessarily band-limited) is identified using input signal of the analog system the Dirac impulse. The impulse response of the analog system is sampled to produce the impulse response of the digital system.

for $x_a(t)=\delta(t)\Rightarrow y_a(t)=h_a(t)$; $x_d[n]=\frac{1}{T}\delta[n]$; $y_a(nT)=h_a(nT)$.

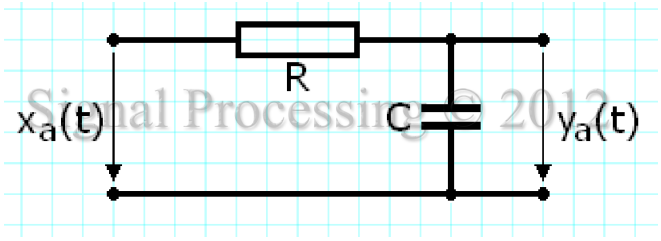
$$y_d[n]=\frac{1}{T}\delta[n]*h_d[n]=\frac{1}{T}h_d[n]$$

The error is smallest for: $h_d[n]=Th_a(nT)$

The frequency response of the digital system is the same with the frequency response of the analog system of limited band for frequency less than half of the sampling frequency

$$H_a(\omega) = H_d(\Omega)\big|_{\Omega=\omega T};\quad |\omega| \le \frac{\pi}{T} \text{ and } \omega_M \le \frac{\pi}{T}$$

7. *Approximation of RC circuit using bilinear transform method.*



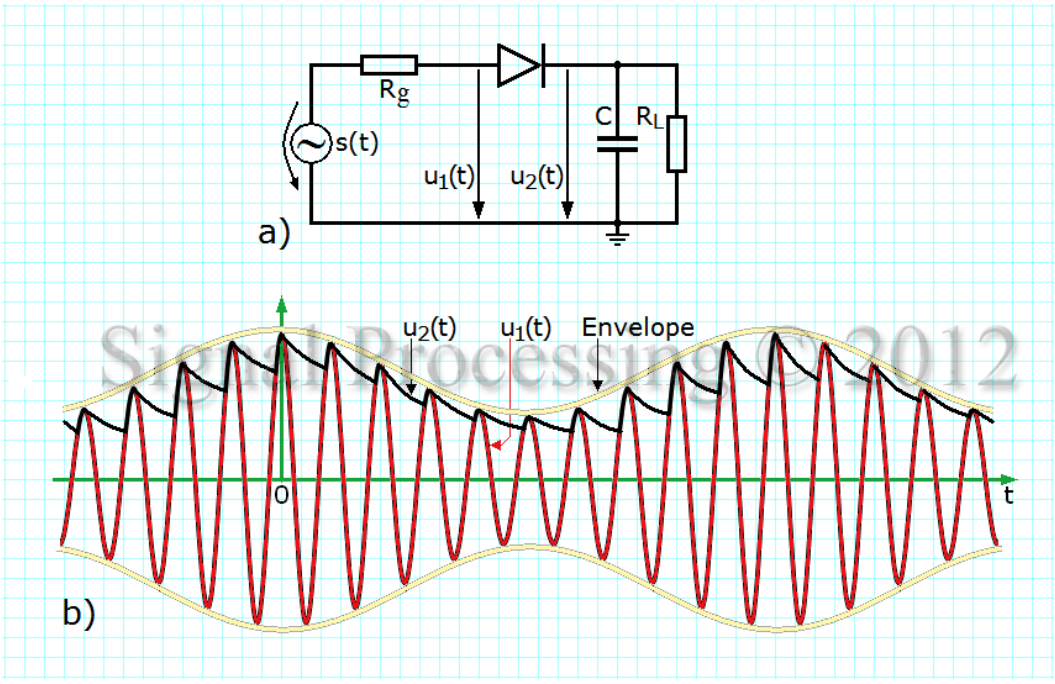
time constant: $\tau = RC = \frac{1}{\omega_0};\quad H_a(s) = \frac{1}{1+s\tau}$

$$s = \frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}};\qquad H_d(z) = H_a(s)\Big|_{s=\frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}}}$$

$$\Rightarrow H_d(z) = \frac{\frac{T}{T+\tau}}{1-\frac{\tau}{T+\tau}z^{-1}}$$

8. *Demodulator (envelope detector) for AM signals.*

AM demodulation can be realized using an envelope detector. For $R_g << R_s$, the voltage from the capacitor $u_2(t)$ follows the voltage $u_1(t)$ if the latter is high enough and the diode conducts (on the positive half-cycle of the input signal). When the diode becomes reverse biased, the capacitor discharges through the resistor R_L. The modulating wave is reconstructed using low pass filtering and removal of the DC component for $u_2(t)$.



9. *Narrow Band Frequency Modulation.*

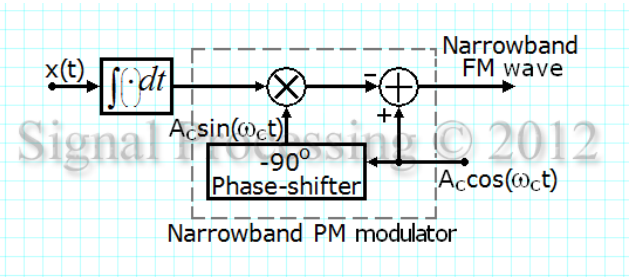
FM signal's expression is: $s(t) = A_c \cos\theta_i(t) = A_c \cos\left[\omega_c t + \beta \sin \omega_m t\right]$, where the modulating wave to be transmitted is $x(t) = A_m \cos \omega_m t$. Depending on the value of the modulation index $\beta = \Delta\omega / \omega_m$, we have narrow band FM ($\beta << 1$ radian) or wide band FM ($\beta >> 1$ radian). For narrow band FM, the modulated wave is:

$$s(t) = A_c \cos\omega_c t \cos(\beta \sin \omega_m t) - A_c \sin\omega_c t \sin(\beta \sin \omega_m t).$$

If $\beta < \dfrac{\pi}{36}$ rad $\Rightarrow \cos(\beta \sin \omega_m t) \cong 1$ and $\sin(\beta \sin \omega_m t) \cong \beta \sin \omega_m t$

$$\Rightarrow s(t) = A_c \cos\omega_c t - \beta A_c \sin\omega_c t \sin\omega_m t.$$

A possible implementation scheme is shown below.

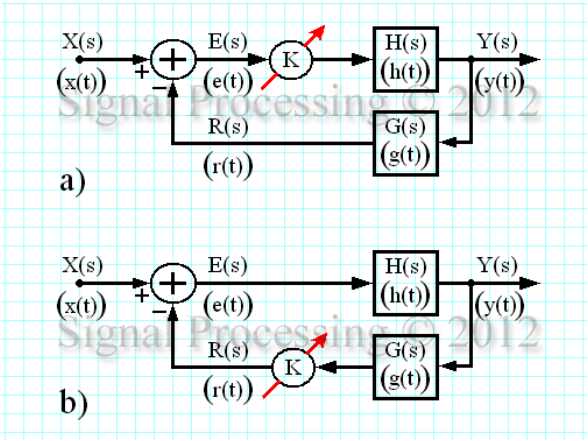


There are two disadvantages:

1-the envelope is affected by residual amplitude modulation so it varies in time,

2-for a harmonic modulating wave, the angle $\theta_i(t)$ contains other harmonics (order 3 and superior) of the modulating frequency, ω_m, so it is distorted.

10. Nyquist stability criterion for continuous-time systems when the open loop system is stable (schema + enunciation).



a) $$\frac{Y(s)}{X(s)} = \frac{KH(s)}{1+KH(s)G(s)}$$

b) $$\frac{Y(s)}{X(s)} = \frac{H(s)}{1+KH(s)G(s)}$$

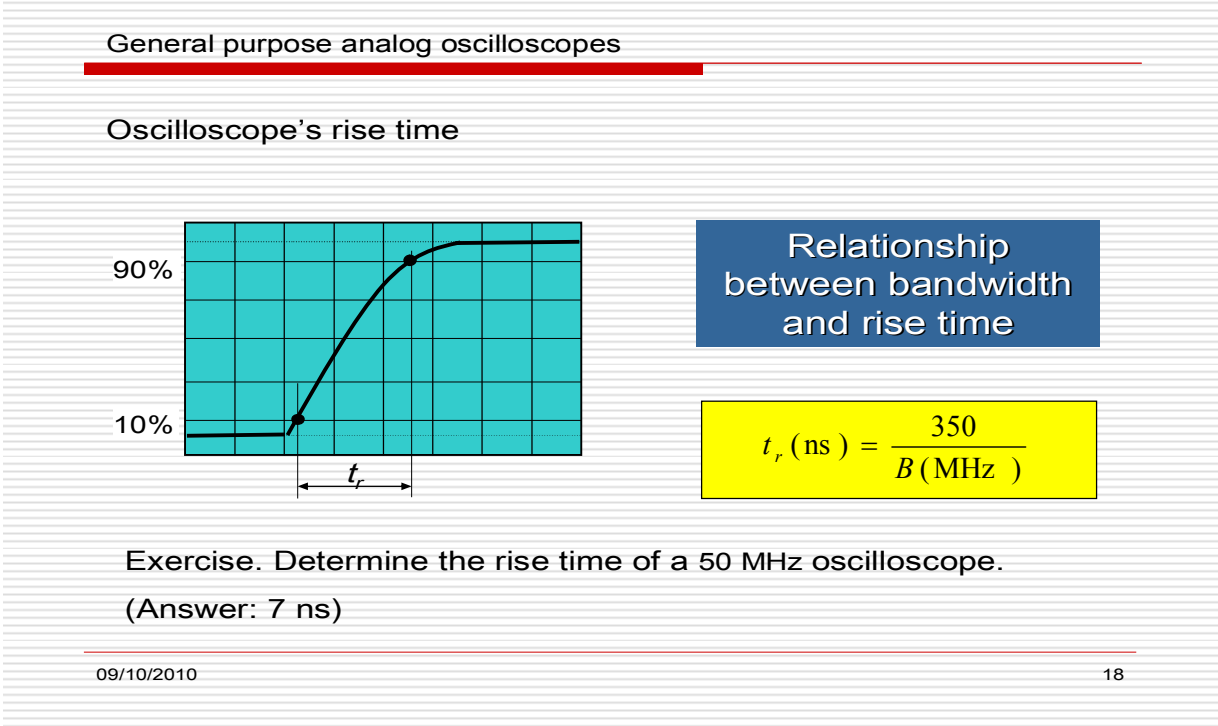
-If the open loop system is stable then $H(s)G(s)$ doesn't have poles in the right half plane or on the imaginary axis. So, the open loop Nyquist's hodograph G(jω)H(jω) **doesn't make complete rotations** around the point (-1/K,0)

-Since $h(t)$ and $g(t)$ are real functions, Nyquist's hodograph for $\omega \in (-\infty,0)$ is obtained by **symmetry** with respect to the real axis of the complex plane $H(s)G(s)$ from the Nyquist's hodograph for $\omega \in (0,\infty)$

Electronic Instrumentation

1. ***General purpose analog oscilloscopes. Relationship between bandwidth and rise time of an oscilloscope. Determine the rise time of a 20 MHz oscilloscope.***

https://intranet.etc.upt.ro/~E_INSTR/PowerPoint%20presentations%202010%202011/1%20Oscilloscopes%202010%202011.ppt , slide #18

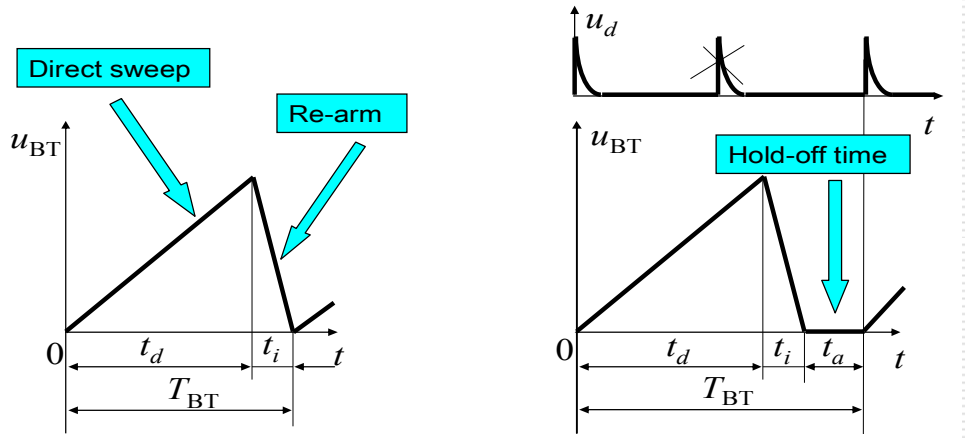


Answer: The rise time of a 20 MHz oscilloscope is 17 ns.

2. ***General purpose analog oscilloscopes. Describe the free-running and the triggered modes of operation of the time base.***

https://intranet.etc.upt.ro/~E_INSTR/PowerPoint%20presentations%202010%202011/1%20Oscilloscopes%202010%202011.ppt, slides #33-38

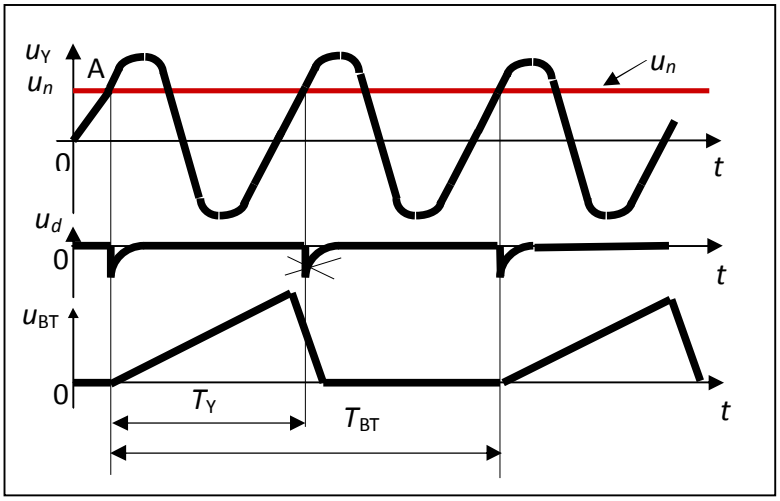
Sweep generator – two operating modes: free-running and triggered

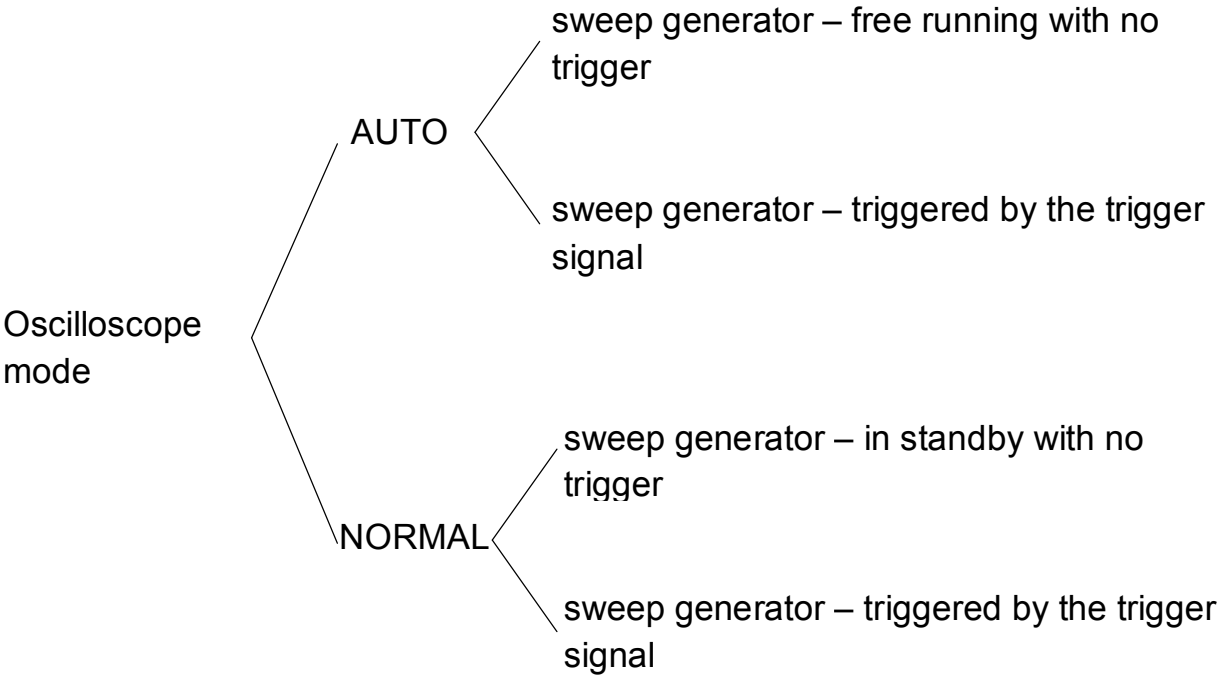


With triggered sweeps, the scope will blank the beam and start to reset the sweep circuit (re-arm) each time the beam reaches the extreme right side of the screen. For a period of time, called *hold-off*, the sweep circuit resets completely and ignores triggers. Once hold-off expires, the next trigger starts a sweep. The trigger event is usually the input waveform reaching some user-specified threshold voltage (trigger level) in the specified direction (going positive or going negative - trigger polarity). Triggering circuit ensures a stable image on the screen.

Triggering condition $T_{BT} = kT_Y$

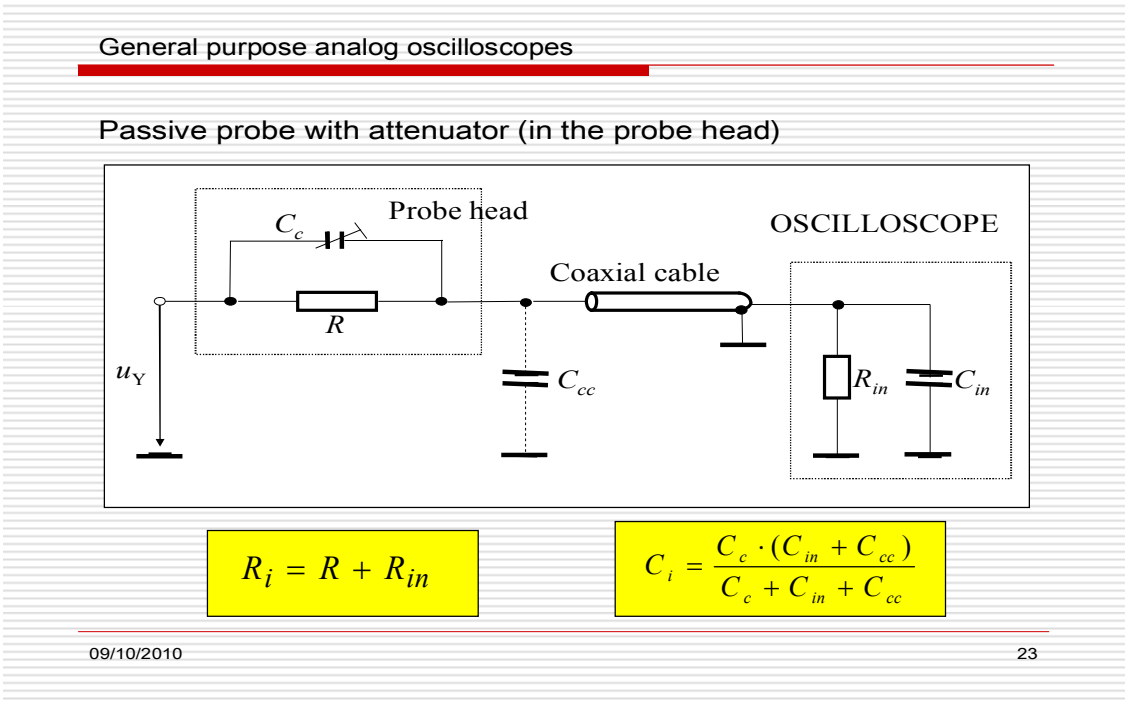
The sweep generator's period should be a multiple of the signal period. Timing diagrams (triggered sweep):





3. ***Probes for oscilloscopes. Attenuating probes. Frequency compensation. Describe what happens and tell (and draw) how the image of square pulses appears on the screen when the compensation condition is not met.***

https://intranet.etc.upt.ro/~E_INSTR/PowerPoint%20presentations%202010%202011/1%20Oscilloscopes%202010%202011.ppt, slides #23-25



Probes without and with attenuator - comparison

Probe without attenuator

- advantage – it does not attenuate the input signal
- disadvantage – relatively small input resistance (1 MΩ), large input capacitance (50 - 150 pF)

Probe with attenuator

- advantage – large input resistance (10 MΩ), small input capacitance (5 - 15 pF)
- disadvantage – it attenuates the input signal (therefore, the value read on the display must be multiplied by the probe's attenuation factor)

4. *General purpose analog oscilloscopes. Delayed sweep: use, operating modes, utility.*

https://intranet.etc.upt.ro/~E_INSTR/PowerPoint%20presentations%202010%202011/1%20Oscilloscopes%202010%202011.ppt, slides #48-50

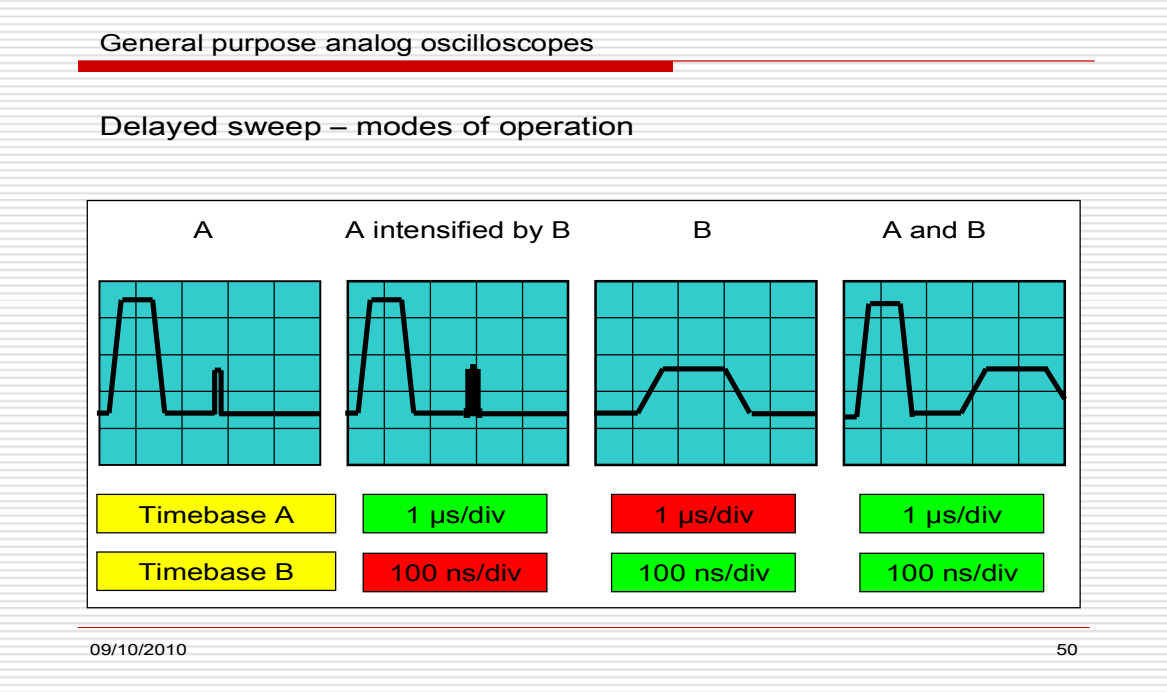
Delayed sweep

- found on more-sophisticated oscilloscopes, which contain a second set of timebase circuits for a delayed sweep.
- provides a very-detailed look at some small selected portion of the main timebase.

The main timebase serves as a controllable delay, after which the delayed timebase starts. This can start when the delay expires, or can be triggered (only) after the delay expires. Ordinarily, the delayed timebase is set for a faster sweep, sometimes much faster, such as 1000:1. At extreme ratios, jitter in the delays on consecutive main sweeps degrades the display, but delayed-sweep triggers can overcome that.

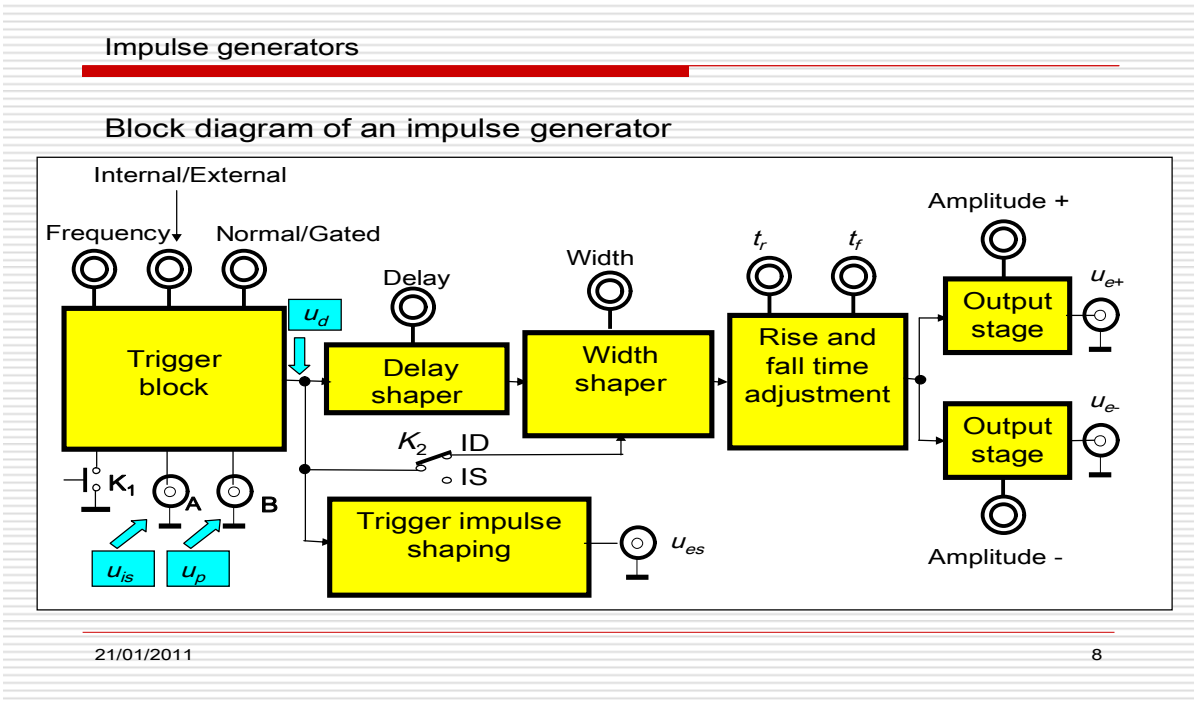
Operating modes

- A
- A intensified by B
- B
- A and B (mixed)



5. *Signal generators. Describe the operation of the pulse generator in single and double pulses modes.*

https://intranet.etc.upt.ro/~E_INSTR/PowerPoint%20presentations%202010%202011/2%20Signal%20Generators%202010%202011.ppt, slides #8-11



Operating modes

1. NORMAL

- ❑ internally triggered (simple or double impulses)
- ❑ externally triggered (simple or double impulses)
- ❑ single impulses (simple or double impulses)

2. GATED

- ❑ simple or double impulses

Operating modes

Normal, internally triggered, simple positive impulses

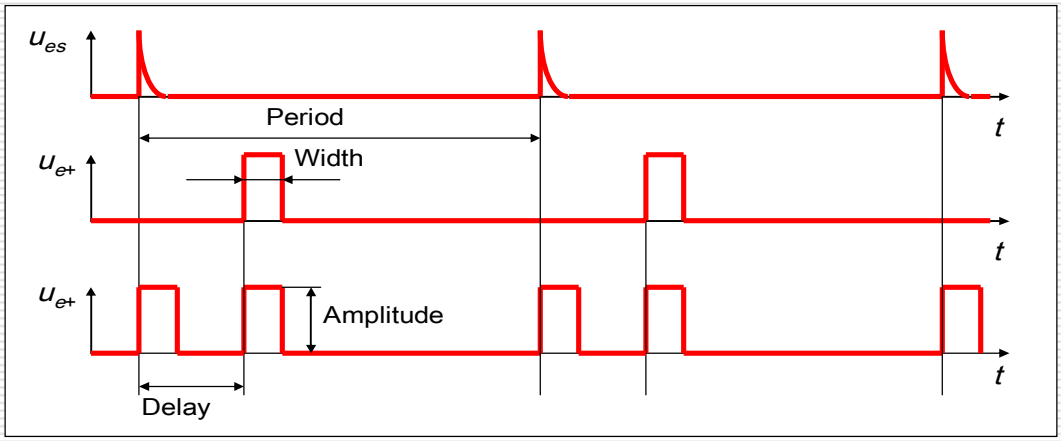
The trigger block operates autonomously and sets the repetition rate of the generated impulses.

The generator provides, in each cycle, a trigger pulse and one pulse at each output (positive and negative), delayed with respect to the trigger pulse.

Impulse generators

Operating modes

Normal, internally (or externally) triggered, simple or double positive impulses



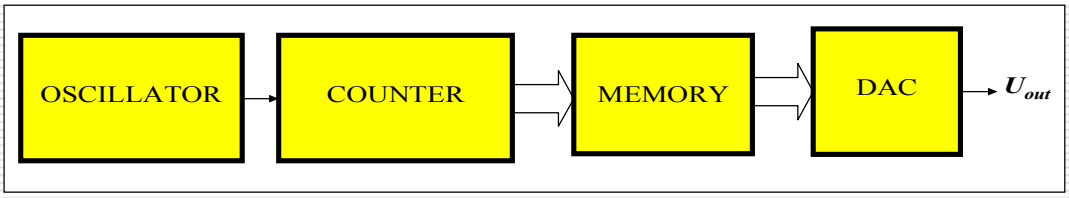
21/01/2011 11

6. *Signal generators. Describe the operation principle of a Direct Digital Synthesis generator.*

https://intranet.etc.upt.ro/~E_INSTR/PowerPoint%20presentations%202010%202011/2%20Signal%20Generators%202010%202011.ppt, slides #35-36

Sine wave generators

Direct digital synthesis generators

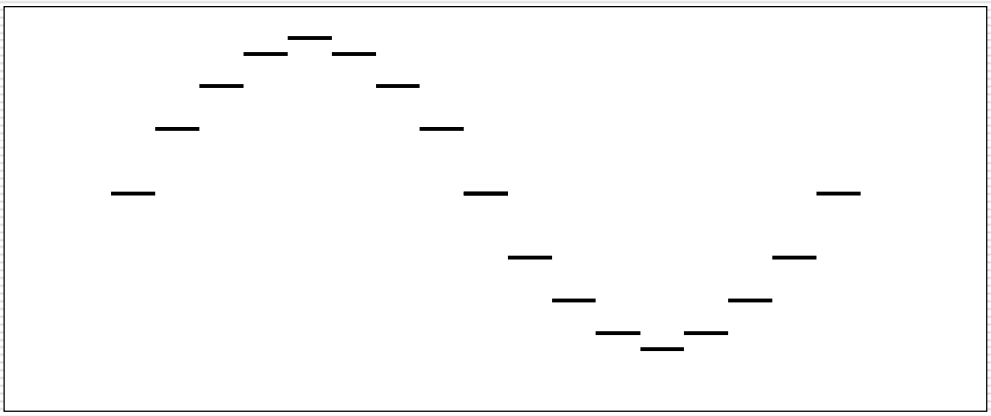


Oscillator (clock generator) – frequency f_0
Counter – n bits (0 - 2^n-1) = memory address
Stored values: $\sin(2\pi i/2^n)$
Output frequency: $f_0/2^n$

21/01/2011 35

Sine wave generators

Direct digital synthesis generators - example (n=4)



21/01/2011 36

7. ***Digital voltmeters and multimeters. Specify the measurement result for a 100% confidence level (result ± uncertainty, confidence level) according to the rules for data presentation when measuring a voltage of 12.45 V with a 3 ½ digit 20 V voltmeter whose maximum permissible error is given by***

$$\Delta_t = 0{,}1\% \times \text{reading} + 0{,}05\% \times \text{range} + 1 \text{ digit}$$

https://intranet.etc.upt.ro/~E_INSTR/PowerPoint%20presentations%202010%202011/3%20Digital%20Voltmeters%20and%20Multimeters%202010%202011.ppt, slides #7-10

Introduction

The maximum permissible error

Δ_t=a% × reading + b% × range + n digits

Δ_t=a% × reading + c% × range

Δ_t=a% × reading + m digits

Remark. One digit represents one LSD.

Example. One digit is 1 mV in case of a 2 V, $3^1/_2$ digit DVM (readout x,xxx V).

21/01/2011 7

Introduction

Data presentation rules

1. Measurement error and uncertainty should be expressed with no more than two significant digits.
2. The LSD of the measurement result and of its corresponding error/uncertainty should have the same weight.

Examples.

Right	Wrong
0,2%	0,256%
3,5 mV	3,58 mV
0,02 mA	0,0222 mA

Right	Wrong
1,0 ± 0,2 mA	1 ± 0,2 mA
1,538 V ± 0,003 V	1,538 V ± 0,03 V
1,538 V ± 3 mV	1,53 V ± 3 mV

21/01/2011 8

Exercise. The maximum permissible error of a 20V, $3^{1/2}$ digit DVM is given by

$$\Delta t = 0{,}1\% \times \text{reading} + 0{,}05\% \times \text{range} + 1 \text{ digit}$$

Determine the uncertainty for a measured value of 12.45 V and specify the measurement result corresponding to a confidence level of 100%.

Present the other two forms of the maximum permissible error.

Solution. The DVM reads xx,xx V. Therefore,

1 digit = 10 mV.

The maximum permissible error when measuring 12.45 V is

$\Delta t = 0{,}1\% \times 12.45 \text{ V} + 0{,}05\% \times 20 \text{ V} + 10 \text{ mV}$,

or

$\Delta t = 32.45 \text{ mV} \cong 30 \text{ mV}$.

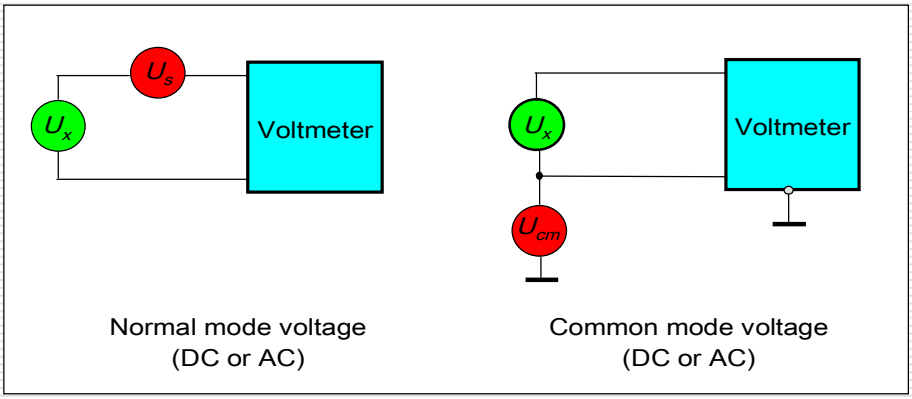
For a confidence level of 100%, the measurement result should be specified as

$U = 12.45 \text{ V} \pm 30 \text{ mV}$.

8. *Digital voltmeters and multimeters. Define normal and common mode voltages and the respective rejection ratios (NMRR and CMRR)*

https://intranet.etc.upt.ro/~E_INSTR/PowerPoint%20presentations%202010%202011/3%20Digital%20Voltmeters%20and%20Multimeters%202010%202011.ppt, slides #20, 23, 28

Measurement errors due to external noise



Normal mode voltage
(DC or AC)

Common mode voltage
(DC or AC)

The ability of a DC DVM to reject an AC normal mode signal is described by the Normal Mode Rejection Ratio (acronym NMRR):

$$NMRR = \frac{\text{amplitude of the normal mode voltage}}{\text{equivalent DC voltage}}$$

Example. For a DC DVM with a NMRR of 100, a normal mode voltage with an amplitude of 1 V produces an additional error of

1 V/100 = 0,01 V = 10 mV.

DC digital voltmeters

The ability of a DC DVM to reject a common mode signal is described by Common Mode Rejection Ratio (acronym CMRR):

$$CMRR = \frac{\text{tensiunea perturbato are de mod comun}}{\text{tensiunea serie echivalent ă}}$$

Aplicație. Un voltmetru de tensiune continuă are CMRR = 1000. O tensiune de mod comun de 5 V conduce la o tensiune serie echivalentă de 5 V/1000 = 5 mV.

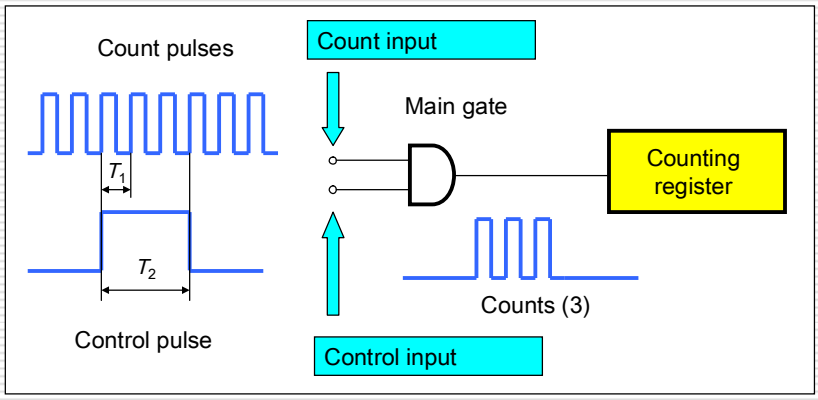
21/01/2011 28

9. *Universal counters. Describe the operating principle and explain how frequency can be measured.*

https://intranet.etc.upt.ro/~E_INSTR/PowerPoint%20presentations%202010%202011/4%20Universal%20counters%202010%202011.ppt, slides #6-10

Universal counters

Operating principle



02/12/2010 6

Displayed result:

$$N_x = \frac{T_2}{T_1}$$ or $$N_x = f_1 T_2$$

Frequency measurement

The frequency f of a repetitive signal can be defined by the number of cycles of that signal per unit of time

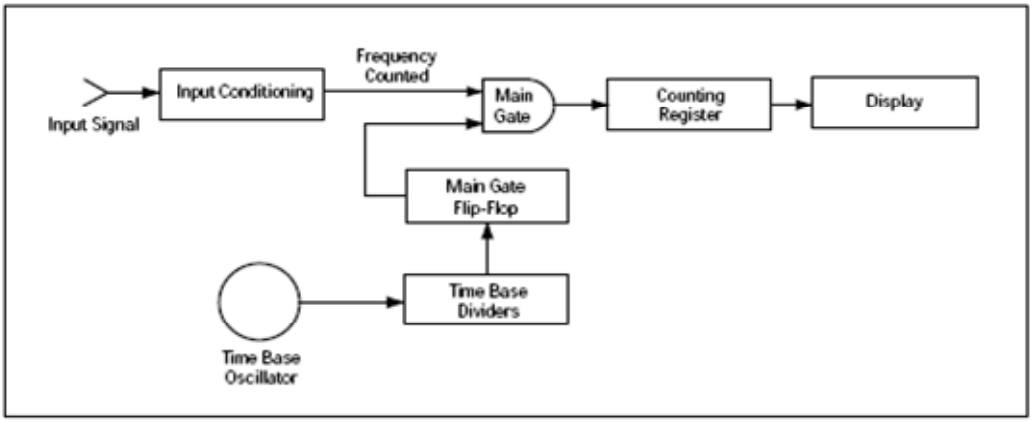
f=n/t,

where n is the number of cycles and t is the time interval in which they occur. As suggested by the above equation, the frequency can be measured by counting the number of cycles and dividing it by t. By taking t equal to one second, the number of counted cycles will represent the frequency (in Hz) of the signal.

The input signal is initially conditioned to a form that is compatible with the internal circuitry of the counter. The conditioned signal is a pulse train where each pulse corresponds to a cycle of the input signal. With the main gate open, pulses are allowed to pass through and get totalized by the counting register.

Universal counters

Basic block diagram of a universal counter in the frequency measurement mode



The time base oscillator together with the decade dividers and the main gate flip flop control the opening time of the main gate.

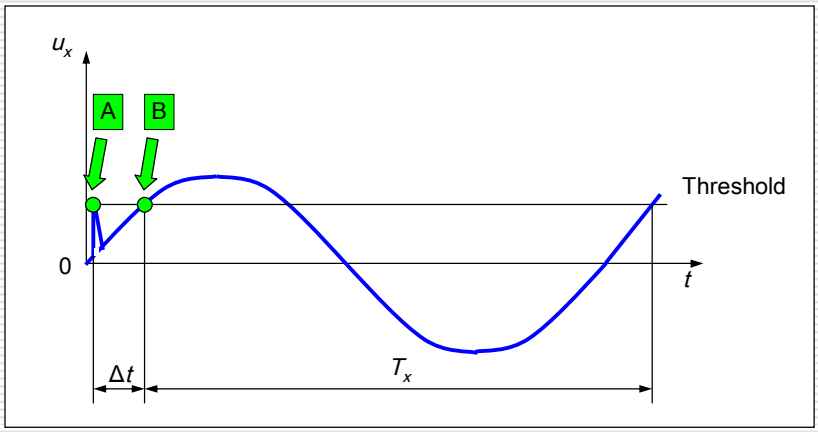
02/12/2010 10

10. *Universal counters. Trigger error for period measurements.*

https://intranet.etc.upt.ro/~E_INSTR/PowerPoint%20presentations%202010%202011/4%20Universal%20counters%202010%202011.ppt, slides #24-26

Errors of universal counters

Period measurement – trigger error



02/12/2010 24

Errors of universal counters

Trigger error

- for single period measurement

$$\delta_b = \frac{1}{\pi \cdot S/Z}$$

S/Z = signal to noise ratio

- for multiple period averaging

$$\delta_b = \frac{1}{N \cdot \pi \cdot S/Z}$$

02/12/2010 25

Errors of universal counters

Measurement uncertainty

- frequency meaurement

$$\delta_{fx\lim} = \delta_c + \delta_{osc}$$

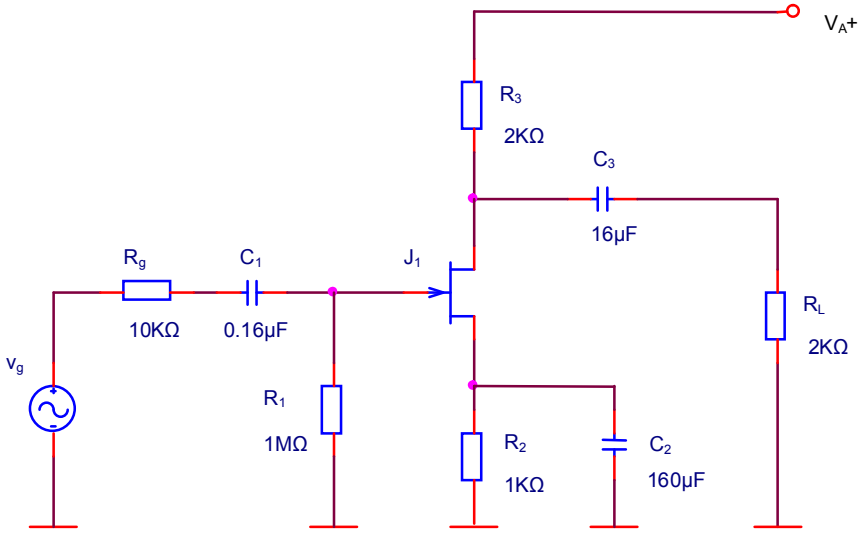
- period measurement

$$\delta_{Tx\lim} = \delta_c + \delta_{osc} + \delta_b$$

Fifth thematic area (apps)

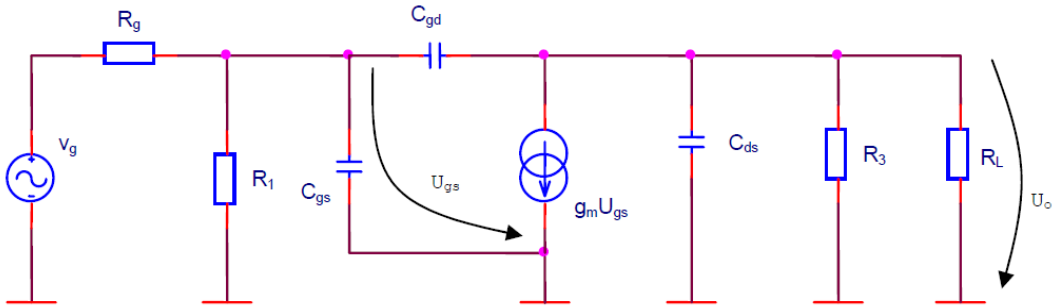
Electronic Circuits

1. **For the circuit below, having the J-FET with parameters: $g_m = 5mA/V$, $r_{ds} = \infty$, $C_{gd} = 5pF$, $C_{gs} = 10pF$, $C_{ds} = 10pF$.**
   Find out the high cutt off frequency by:
   a) Using Miller Theorem;
   b) Using OCTC (Open Circuit Time Constant) method.

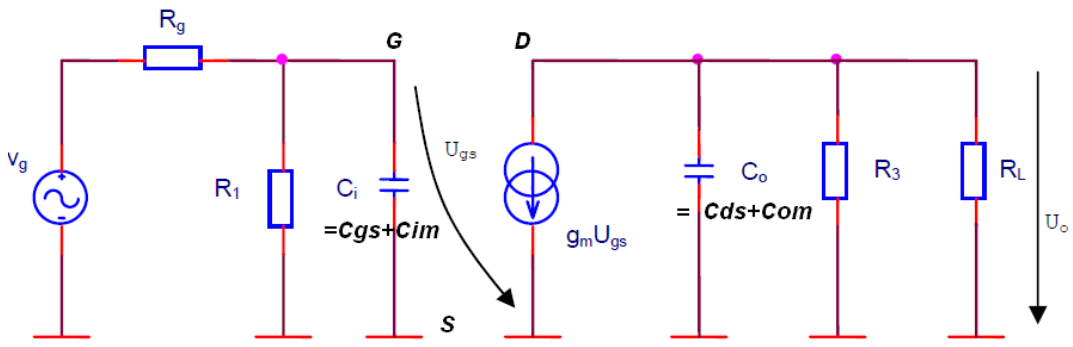


Solution:

a) First must draw equivalent schematic for small signal, mean frequencies:



By using Miller theorem, Cgd cand be splitted in 2 capacitors to ground Cim and Com, which will add to existing Cgs respective Cds, resulting in Ci and Co as below:



Gain *K* between G and D is needed to estimate Cim and Com capacitances:

$$K = \frac{U_o}{U_i} \text{ şi } U_o = -g_m U_{gs}(R_3 \| R_L),\ U_i = U_{gs} \Rightarrow K = A_{U0} = -g_{ms} R_3 \| R_L = -5$$

Then according to Miller:

$$C_{iM} = C_{gd}(1-K) = 30 \text{ pF},\ C_{oM} = C_{gd}\left(1 - \frac{1}{K}\right) = 6 \text{ pF}$$

$$C_i = C_{gs} \| C_{iM} = C_{gs} + C_{iM} = 40 \text{ pF},\ C_o = C_{ds} \| C_{oM} = C_{ds} + C_{oM} = 16 \text{ pF}$$

Cutt of (pole) frequencies introdeced by these capacitors are:

$$f_{P1} = \frac{1}{2 \cdot \pi \cdot C_i \cdot R_{P1}},\ R_{P1} = R_g \| R_1 \cong R_g \cong 10K\Omega \Rightarrow f_{P1} = 400KHz$$

$$f_{P2} = \frac{1}{2 \cdot \pi \cdot C_o \cdot R_{P2}},\ R_{P2} = R_3 \| R_L = 1K\Omega \Rightarrow f_{P2} = 10MHz\ .$$

Transfer function by neglecting zero frequency introduced by Cgs will be:

$$A_U(j\omega) = -5 \cdot \frac{1}{(1 + j\frac{f}{0.4 \cdot 10^6}) \cdot (1 + j\frac{f}{10 \cdot 10^6})}$$

High cutt of frequency will have aproximative value:

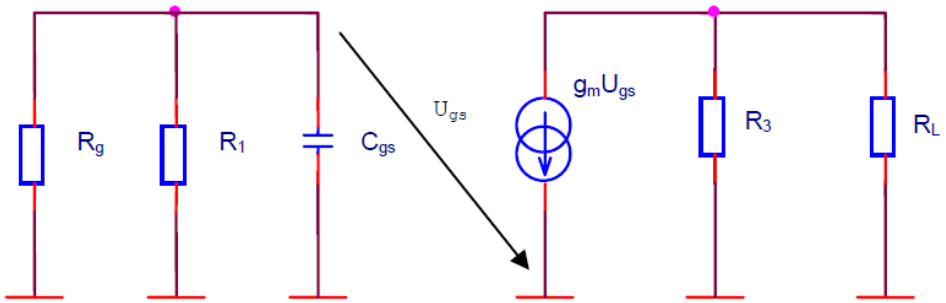
$$f_{P1} = 400\text{KHz}$$

Or can be computed exactly considering the 3db attenuation at cutt of frequency:

$$\left|A_U(j\omega)\right|_{f=f_{\hat{i}}} = \frac{1}{\sqrt{2}} A_{U0} \Rightarrow f_{\hat{i}} = 393{,}7\text{KHz}$$

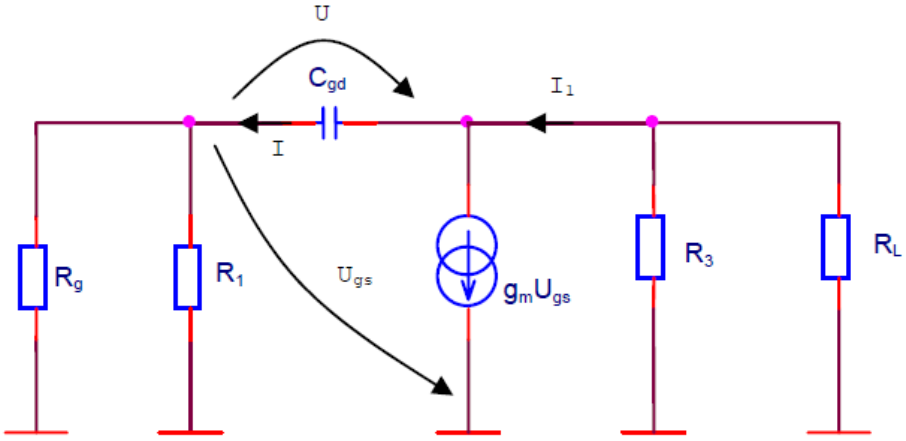
b) If OCTC is applied to first schematic (without to get benefit of Miller theoreme), involve to evaluate 3 time constants, one for each capacitor as folows:

- **Cgs effect**, all the others C = open circuit:



$$f_{P1} = \frac{1}{2 \cdot \pi \cdot C_{gs} \cdot R_{P1}}, R_{P1} = R_1 \| R_g \cong R_g \cong 10K \Rightarrow f_{P1} = 1{,}6MHz$$

- **Cgd effect**, all the others C = open circuit:



$$f_{P2} = \frac{1}{2 \cdot \pi \cdot C_{gd} \cdot R_{P2}}$$

Equivalent resistance between Cgd nodes can be found if Cgd is replaced with a voltage source U:

$$R_{P2} = \left| \frac{U}{I} \right|$$

Using Kirchhoff laws :

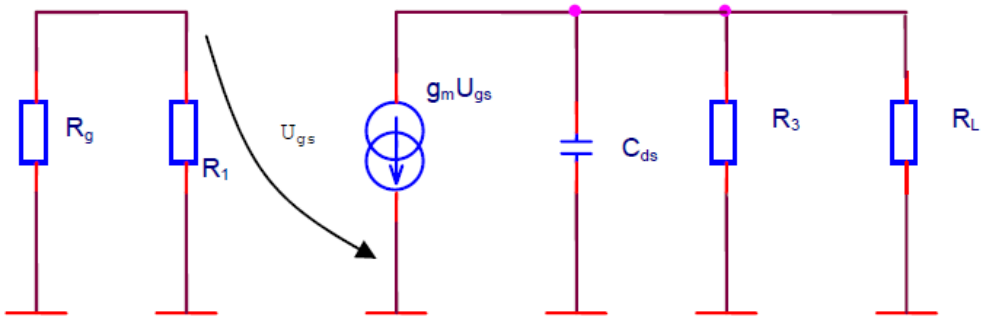
$$-i \cdot R_g \| R_1 + u_{gs} = 0 \Rightarrow u_{gs} = i \cdot R_g \| R_1$$

$$I_1 = g_m \cdot u_{gs} + I = I(1 + g_m \cdot R_g \| R_1)$$

$$U - I \cdot R_g \| R_1 - I_1 \cdot R_3 \| R_L = 0 \Rightarrow U = I \cdot R_g \| R_1 + I \cdot (1 + g_m \cdot R_g \| R_1) \cdot R_3 \| R_L$$

$$R_{P2} = \frac{U}{I} = R_g \| R_1 + (1 + g_m \cdot R_g \| R_1) \cdot R_3 \| R_L = 61\text{K}\Omega. \Rightarrow f_{P2} = 524{,}6KHz$$

- **Cds effect**, all the others C = open circuit:



$$f_{P3} = \frac{1}{2 \cdot \pi \cdot C_{ds} \cdot R_{P3}},\ R_{P3} = R_3 \| R_L = 1K \Rightarrow f_{P3} = 16MHz$$

According to SCTC:

$$\frac{1}{f_i} = \frac{1}{f_{i1}} + \frac{1}{f_{i2}} + \frac{1}{f_{i3}} \Rightarrow f_i \cong 385{,}2KHz.$$

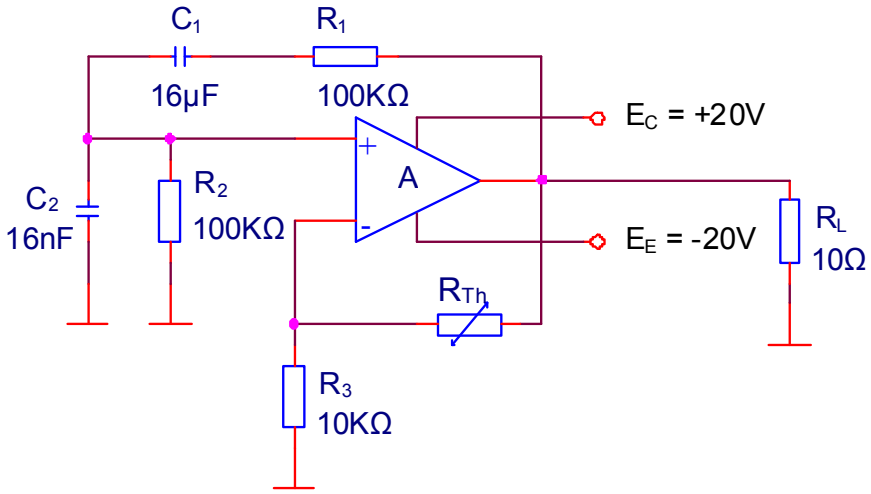
close to the value obtained at a)

2. **The schematic below is a Wien oscillator using a class B final stage amplifier having: $A_u \to \infty$, $R_i \to \infty$, $R_o \to 0$. Find out:**

a) f_0 oscillating frequency,

b) V_0, when using the thermistor R_{Th};

c) P_0 (delivered to R_L)



Solution:

a) $f_o = \dfrac{1}{2 \cdot \pi \cdot \sqrt{R_1 R_2 C_1 C_2}} \cong 100Hz$

b) $A = 1 + R_{Th}/R_3$, and at f_0: $|\beta| = 1/3$.

From $|A||\beta| = 1 \Rightarrow R_{Th} = 20K\Omega$ obtained for $U_{Th} = 10V$.
Feedback topology is series-shunt, actually a voltage divider including R_{Th}, so:

$$u_{Rth} = u_o \cdot \frac{R_{Th}}{R_{Th} + R_3} = \frac{2}{3} \cdot u_o \Rightarrow u_o = 1{,}5 \cdot u_{Rth} = 15V_{ef}$$

$$u_{om} = \sqrt{2} \cdot 15V_{vv}$$

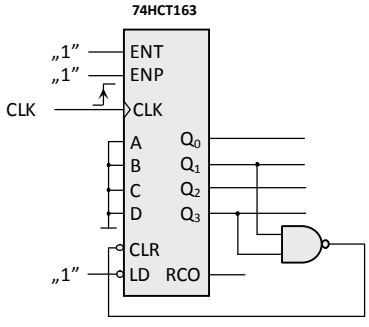
c)

$$P_o = \frac{u_{om}^{\ 2}}{2 \cdot R_L} = 22{,}5W$$

Digital Integrated Circuits

3. Use a 74x163 binary synchronous counter (with synchronous reset) to design a modulus 11 counter (the counting sequence is: 0, 1, 2... 10, 0, 1, 2, ...). Explain what happens if the reset is asynchronous.

Solution: A 2-input NAND gate is used to detect the 10 state ($Q_3Q_2Q_1Q_0$ = 1010) and by clearing the counter the next state will be 0000. A different modulus is obtained if the reset is asynchronous. The Preset inputs (A, B, C, D) and the nLD input are not used.



4. Using 27C256 EPROM memories (32k x 8 bit) and glue logic, design a 64k x 8 bit memory.

Solution: a). The number of EPROM circuits is:

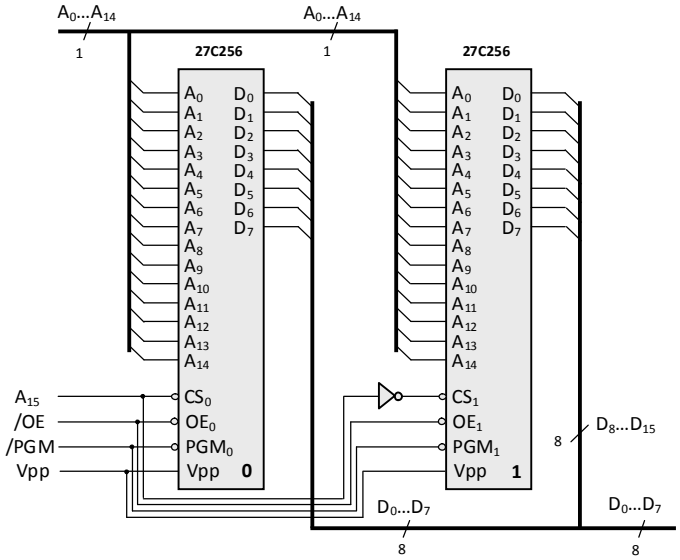
$$N = \frac{64k\,x\,8}{32k\,x\,8} = 2\,.$$

b). The initial memory has 15 address lines ($A_0 \ldots A_{14}$). The final memory has 16 address lines.

A_{15}	$A_{14} - A_0$	Memory #	Enable	
			$\overline{CS_0}$	$\overline{CS_1}$
0	X….. X	0	0	1
1	X….. X	1	1	0

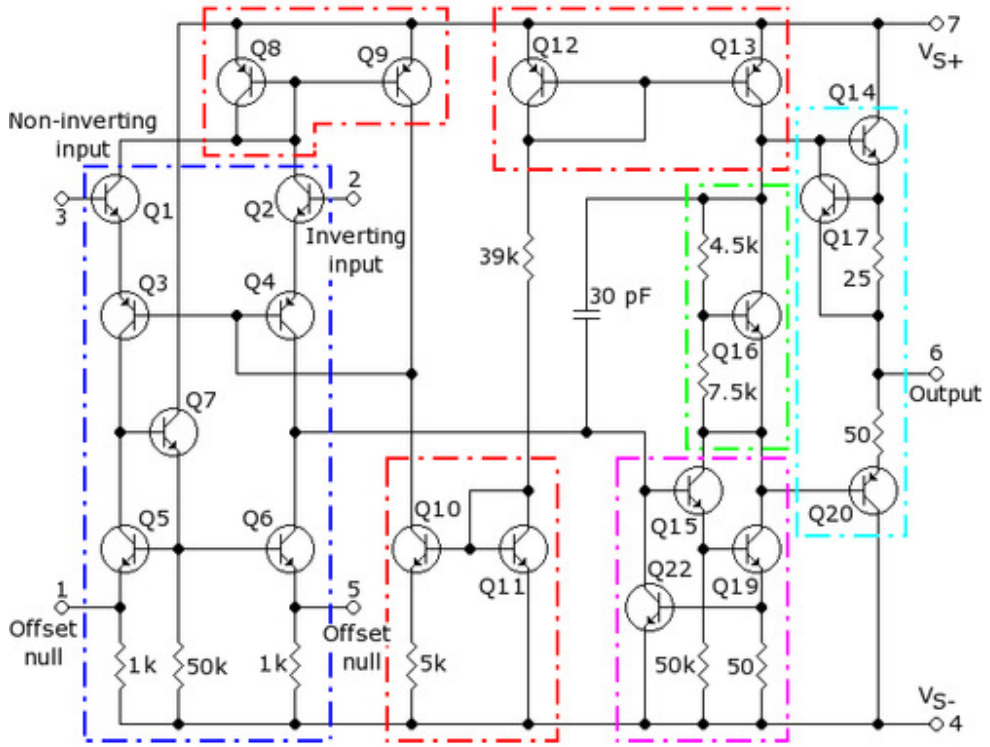
A15 is used to select one of the two memories. One inverter is associated with this task. The two memories have a common address bus $A_0 \ldots A_{14}$ and a common data bus $D_0, \ldots, D_7$. oOE, nPGM and Vpp are also connected together.

The final schematic is:



Analog Integrated Circuits

5. Name the building blocks inside the op. amp. shown in the figure.



Solution:

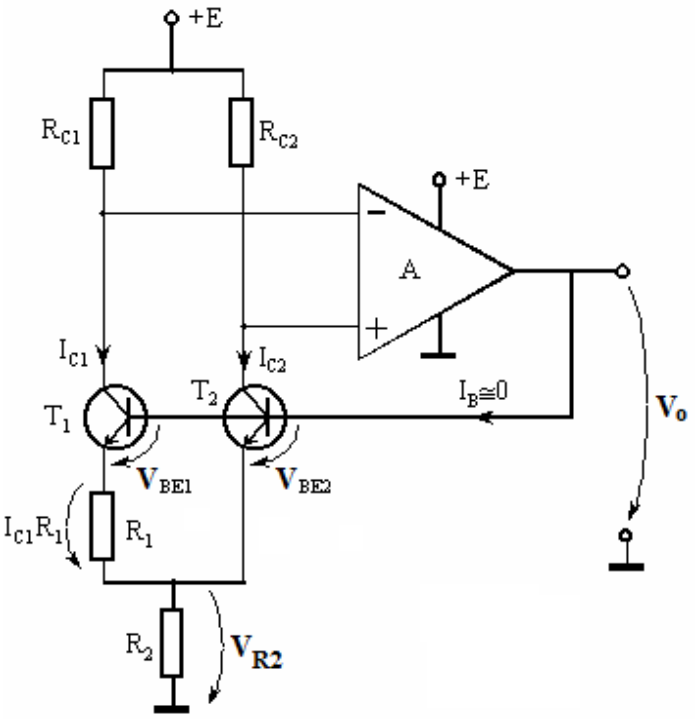
At the left-hand side of the figure, the first block is a differential input stage with emitter followers (*Ql* and *Q2*) driving common-base stages (*Q3* and *Q4*). The transistors *Q5* and *Q6* form an active load for *Q3* and *Q4*. Transistors *Q7*, *Q5*, *Q6* and their emitter resistances form a simple current mirror with degeneration. The two pairs of transistors shown at the top of the schematic are simple current mirrors (*Q8* and *Q9*, *Q12* and *Q13*). At the bottom is a Widlar current source (built by *Q10*, *Q11*, and the 5 kΩ resistor). Transistors *Q15*, *Q19* and *Q22* operate as a class A gain stage. The stage consists of two NPN transistors in a Darlington configuration (*Q15* and *Q19*). Transistor *Q16* and its base resistors is the V_{be} multiplier voltage source. Transistors *Q14*, *Q20* form the class AB push-pull emitter follower output stage.

6. A band-gap-referenced bias circuit is shown in the figure. T_1 and T_2 are identical. The ratio of R_{C1} to R_{C2} is 2: $R_{C1}/R_{C2} = 2$ and $R_1 = 2.6$ KΩ.

a. Calculate the output voltage, V_o and prove that it is possible to have a voltage reference.

b. b). Calculate the value of the currents I_{C1} and I_{C2}.

You have: ln2 = 0.693; ln5 = 1.6; ln10=2.3; V_T=26mV at 300 K.



Solution:

We consider an ideal op. amp. $\Rightarrow \quad V_{R_{C1}} = V_{R_{C2}} \Leftrightarrow I_{C1}R_{C1} = I_{C2}R_{C2} \Rightarrow \dfrac{I_{C2}}{I_{C1}} = \dfrac{R_{C1}}{R_{C2}} = 2 \quad (1)$

KVL in the loop of R_1 and two V_{BE}:

$$V_{BE1} + I_{C1}R_1 = V_{BE2} \Leftrightarrow I_{C1}R_1 = V_{BE2} - V_{BE1} = V_T \ln\frac{I_{C2}}{I_{S2}} - V_T \ln\frac{I_{C1}}{I_{S1}}$$

But T_1 and T_2 are identical $\Rightarrow I_{S1} = I_{S2} \Rightarrow I_{C1}R_1 = V_T \ln\dfrac{I_{C2}}{I_{C1}} = V_T \ln 2 \Rightarrow I_{C_1} = \dfrac{V_T \ln 2}{R_1}$ (2)

$$V_o = V_{BE2} + V_{R_1} = V_{BE2} + (I_{C1} + I_{C2})R_2 \quad (3)$$

$$\overset{(3),(1)}{\Rightarrow} V_o = V_{BE2} + (I_{C1} + 2I_{C1}) \cdot R_2 \overset{(2)}{=} V_{BE2} + 3 \cdot R_2 \cdot \frac{V_T \ln 2}{R_1} = V_{BE2} + \left(3 \cdot \frac{R_2}{R_1} \cdot \ln 2 \right) \cdot V_T$$

V_o will be compensated if $3 \cdot \frac{R_2}{R_1} \cdot \ln 2 = N = 23 \Rightarrow R_2 = \frac{23 \cdot R_1}{3 \cdot \ln 2} \Rightarrow R_2 = \frac{23 \cdot 2.6 \cdot 10^3}{3 \cdot 0.693} = 28.7k\Omega$

So, if $R_2 = 28.7k\Omega$ we have a band-gap referenced circuit and the output voltage is:

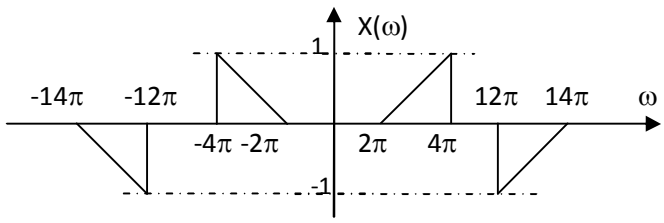
$$V_o = V_{BE} + N \cdot V_T \cong 0.6V + 23 \cdot 26mV = 1.198V$$

b) $I_{C1} = \frac{V_T \ln 2}{R_1} = \frac{26 \cdot 10^{-3} \cdot 0.693}{2.6 \cdot 10^3} \cong 0.7\mu A$

$$I_{C2} = 2 \cdot I_{C1} = 14\mu A$$

Signal Processing

7. Consider the signal $x(t)$ with the spectrum below



What is the minimum sampling frequency $f_{s\min}$ according to the sampling theorem?

Solution:

$$f_{s\min} = 2f_M = 2 \square 7Hz = 14Hz$$

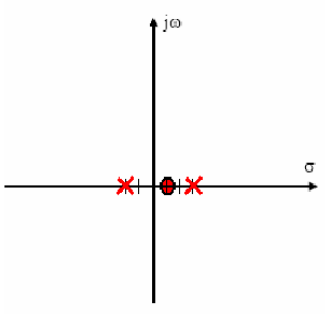
$$f_M = \frac{14\pi rad/s}{2\pi rad} = 7Hz$$

8. **Consider the system with the transfer function** $H(s)=\dfrac{s-1}{(s+2)(s-3)}$.

Sketch its pole/zero plot.

Solution:

$$X(s)=\frac{s-1}{(s+2)(s-3)}$$



x- pole

o – zero

Electronic Instrumentation

9. **The 50 ns rise time of a square wave (t_{ri}) read on the screen of an oscilloscope (t_{ro}) is 60 ns. Determine the oscilloscope's bandwidth! Round it off to the nearest standard value (10, 20, 35, 40, 50, 60, 75, 100, 150, 250, 300, 500 MHz)!**

Solution:

Using the equation $t_{ro}^2=t_{ri}^2+t_r^2$, the rise time of the oscilloscope is found to be

$$\sqrt{3600-2500}=\sqrt{1100}\ \ =33.16ns$$

The bandwidth is

$$B=\frac{350}{t_r}=\frac{350}{33.16}=10.55MHz$$

The nearest standard value is 10 MHz.

10. An universal counter displays 100.100 kHz when measuring the frequency of an input signal. Determine the quantization error in Hz, % and ppm! (remember, "." is the decimal point)

Solution:

The quantization error is 1 Hz (one least significant digit)

or, in percent

$$1 \text{ Hz} / 100100 \text{ Hz} \times 100 = 0.001\%$$

or, in ppm

$$1 \text{ Hz} / 100100 \text{ Hz} \times 1{,}000{,}000 = 10 \text{ ppm.}$$

Radio Communications

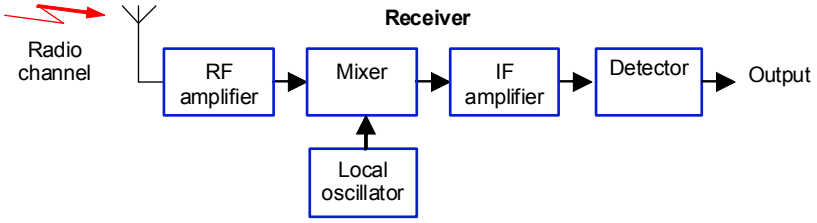
1. Draw and explain the main blocks of a radio receiver.

Course nb.1 slide 12.

Site address: https://intranet.etc.upt.ro/~RADIOCOM/

Answer:

The receiver block incorporate many amplifier and processing stages, and one of the most important is the oscillator stage.



The receiver oscillator is called the local oscillator as it produces a local carrier within the receiver which allows the incoming carrier from the transmitter to be down converted for easier processing within the receiver. The mixer and the IF amplifier are used to extract the intermediate frequency. The user information is obtained after detection.

2. What wavelength corresponds to a frequency of 600 MHz?

Course nb.2 slide 45.

Site address: https://intranet.etc.upt.ro/~RADIOCOM/

Answer:

$\lambda = c/f = (3x10^8 m/s)/(6x10^8 Hz) = 0.5$ m

3. What are the radiation regions of an antenna?

Course nb.3 slide 36-39.

Site address: https://intranet.etc.upt.ro/~RADIOCOM/

Answer:

The antenna radiation field is divided into:

- reactive near-field (objects within this region will result in coupling with the antenna and distortion of the ultimate far-field antenna pattern),

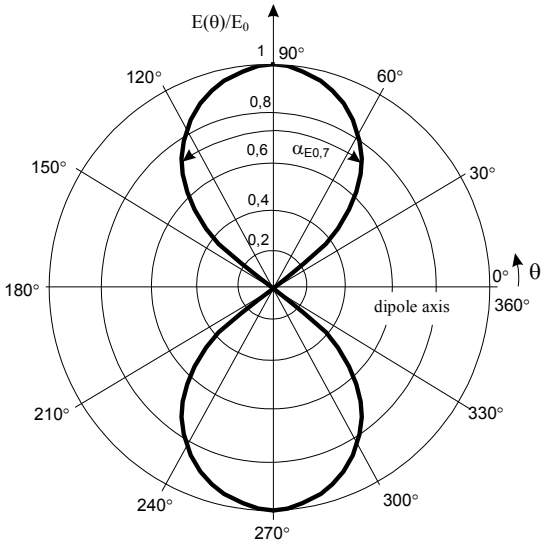
- radiating near-field (transition region),

- far-field (the gain of the antenna is a function only of angle).

4. Describe the directivity of a half-wave dipole antenna.

Course nb.4 slide 35-36.

Site address: https://intranet.etc.upt.ro/~RADIOCOM/



Answer:

A half-wave dipole has an antenna gain of 1.64 or $G = 2.15$ dBi.

It has an Omni directional pattern in the H-plane.

In E-plane the directivity is bidirectional.

5. What represents the array factor?

Course nb.5 slide 15-16.

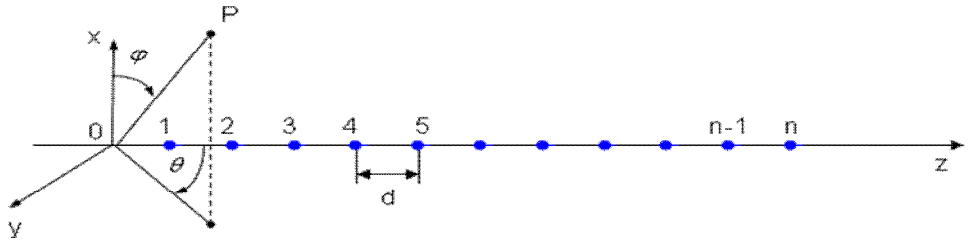
Site address: https://intranet.etc.upt.ro/~RADIOCOM/

Answer:

An array of antennas working simultaneously can focus the reception or transmission of energy in a particular direction, which increases the useful range of a system.

The array influence is contained inside of an array factor AF:

Array pattern = Element pattern x Array factor

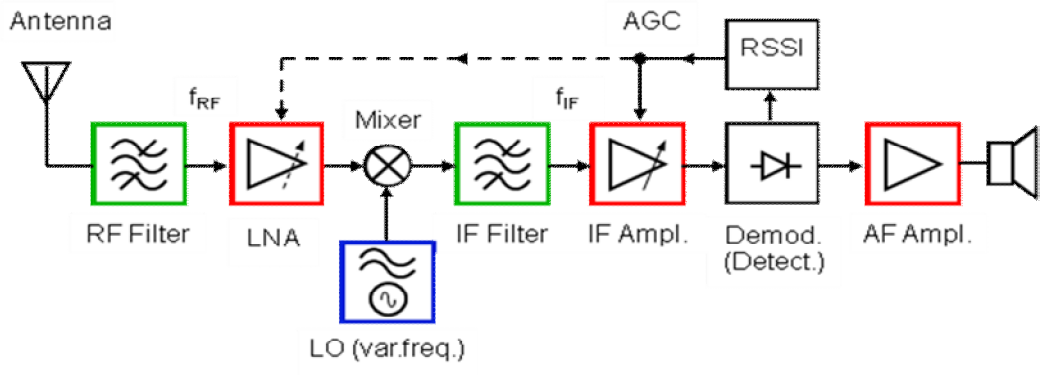


6. Draw and explain the main blocks of a superheterodyne receiver.

Course nb.6 slide 9-11.

Site address: https://intranet.etc.upt.ro/~RADIOCOM/

Answer:



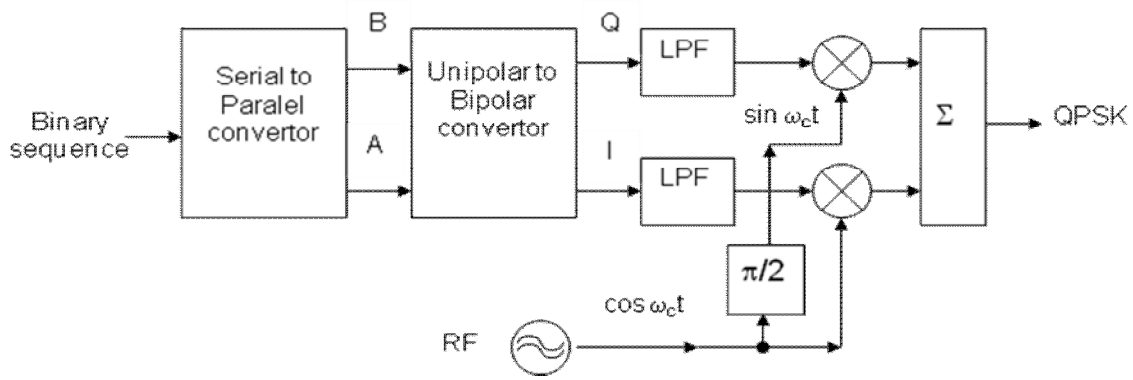
The RF front end consists in a band-pass filter and low-noise amplifier for radio bandwidth selection. The local oscillator and the mixer followed by an IF filter are used for heterodyne process performing channel selection. IF blocks amplify the signal to ensure the right level at the demodulator input. An automatic gain control loop is used to maintain a constant level in case of fading.

7. Draw and explain the QPSK modulator.

Course nb.7 slide 33-34.

Site address: https://intranet.etc.upt.ro/~RADIOCOM/

Answer:



The baseband coding of information consists first in parallel conversion. The two streams resulted are converted in bipolar signals with a symbol duration being twice the bit duration. Each of them is low-pass filtered and used to modulate in phase a RF carrier. The two carriers have a 90^o phase shift to be orthogonal. The result is a constant amplitude signal with 4 possible states of its phasor (4 state constellation).

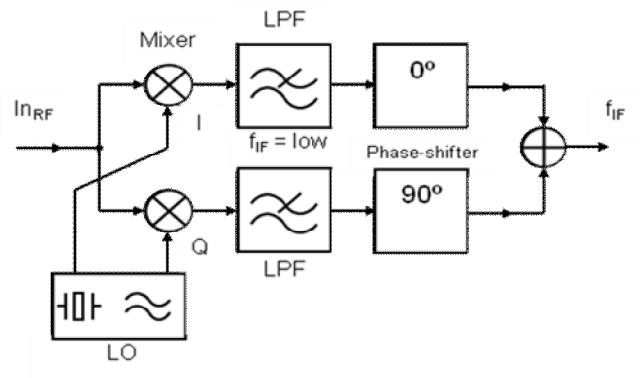
8. Explain the image reject mixer with Hartley architecture.

Course nb.8 slide 17-23.

Site address: https://intranet.etc.upt.ro/~RADIOCOM/

Answer:

The principle of image-rejection is to process the desired channel and its image in such a way that the image can be eliminated eventually by *signal cancellation*.



The RF signal in the downconversion is split into two components by using two matched mixers and quadrature LO signals.

The resulting IF signals, namely in phase (I) and quadrature phase (Q), are then lowpass-filtered and after one is phase-shifted by 90°, the IF signals are combined.

In this process, depending on the IF path that is subjected to the 90° phase-shifter, either the image band or the receive band is cancelled after the summation of I and Q outputs.

9. Define the receiver's selectivity.

Course nb.9 slide 19.

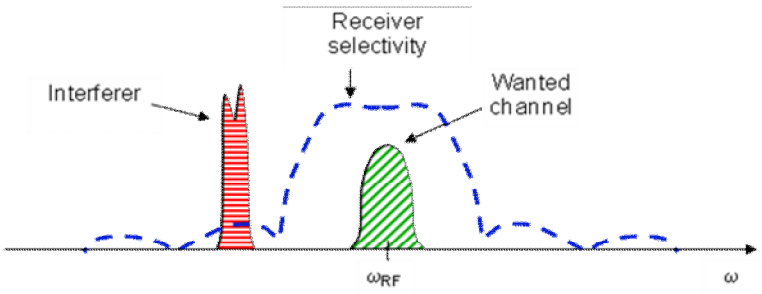
Site address: https://intranet.etc.upt.ro/~RADIOCOM/

Answer:

A receiver's selectivity performance is a measure of the ability to separate the desired band about the carrier, from unwanted interfering signals received at other frequencies.

This situation is most often characterized by a weak received desired signal in the presence of a strong adjacent or alternate band user.

Receiver selectivity may be defined also as the ability to reject unwanted signals on adjacent channel frequencies.



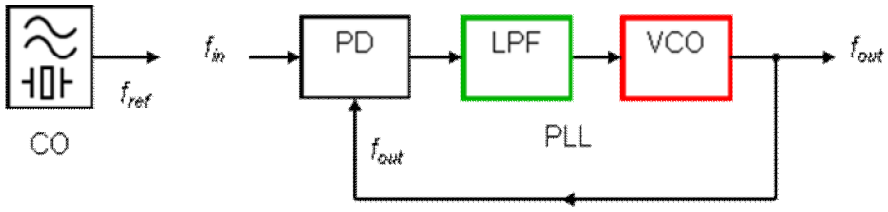
10. Which are the major components of the PLL (Phase-locked loop) frequency synthesizer?

Course nb.10 slide 27-29.

Site address: https://intranet.etc.upt.ro/~RADIOCOM/

Answer:

A PLL is a circuit which causes a particular system to track with another one. More precisely, a PLL is a circuit synchronizing an output signal (generated by an oscillator) with a reference or input signal in frequency as well as in phase.



The major components are the Phase Detector (PD), the LPF = Loop Filter (Low-pass filter LPF), and the Voltage-controlled oscillator (VCO).

Power Electronics

1. *Define the total harmonic distortion coefficient (THD) and the power factor (PF). Power factor formula for sinusoidal input voltage and nonlinear load.*

Given a periodic signal *x(t)*, the *total harmonic distortion coefficient* (THD) is defined as:

$$THD = \frac{rms\ value\ without\ fundamental}{rms\ fundamental} = \frac{\sqrt{X_0^2 + \frac{1}{2}\sum_{n=2}^{\infty} X_n^2}}{\frac{X_1}{\sqrt{2}}}$$

where X_0 is the dc component and X_n are the amplitudes of harmonics.

For efficient transmission of energy from a source to a load, it is desired to *maximize average power*, while *minimizing rms current and voltage* (and hence minimizing losses). The *power factor* (*PF*) is a *figure of merit* that measures how energy is efficiently transmitted. It is defined as the ratio between average power and apparent power:

$$PF = \frac{P}{S}\frac{P}{V_{rms}\cdot I_{rms}} = \frac{\int_{t_0}^{t_0+T} v(t)\cdot i(t)dt}{\sqrt{\frac{1}{T}\int_{t_0}^{t_0+T} v(t)^2 dt}\cdot\sqrt{\frac{1}{T}\int_{t_0}^{t_0+T} i(t)^2 dt}} \qquad (1)$$

With a sinusoidal voltage, current harmonics do not lead to average power. However, current harmonics do increase the rms current, and hence they decrease the power factor.

As with a sinusoidal voltage $P = \frac{1}{2}V_1 I_1 \cos(\varphi_1 - \theta_1)$; $V_{rms} = \frac{V_1}{\sqrt{2}}$; $I_{rms} = \sqrt{I_0^2 + \frac{1}{2}\sum_{n=2}^{\infty} I_n^2}$

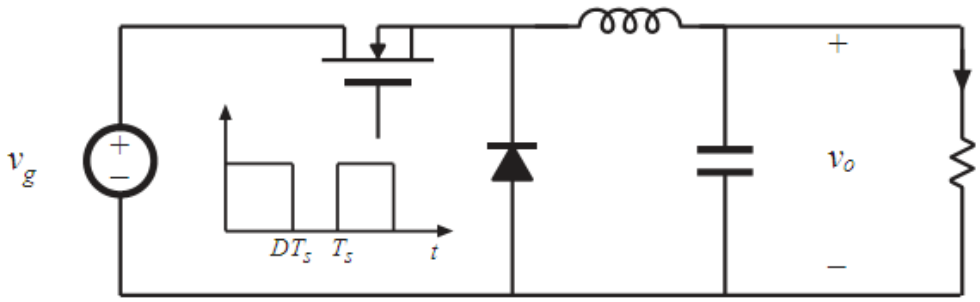
from (1) it results that: $PF = \frac{\frac{I_1}{\sqrt{2}}}{\sqrt{I_0^2 + \frac{1}{2}\sum_{n=2}^{\infty} I_n^2}}\cdot\cos(\varphi_1 - \theta_1) = K_{di}\cdot K_\theta$

where: $K_{di} = \frac{\frac{I_1}{\sqrt{2}}}{\sqrt{I_0^2 + \frac{1}{2}\sum_{n=2}^{\infty} I_n^2}}$ - current distortion factor

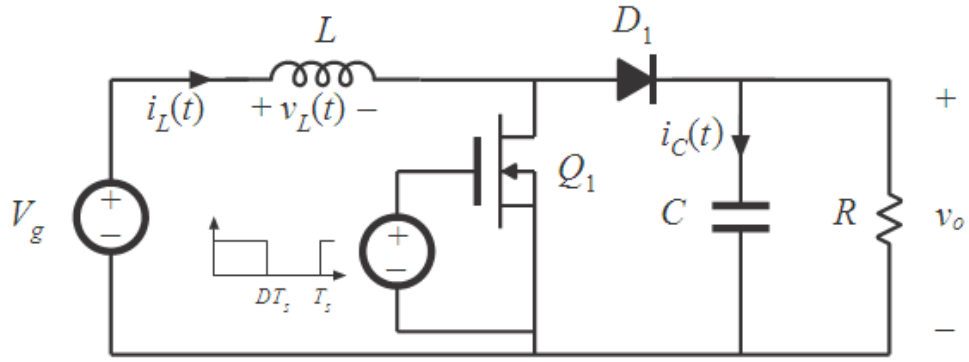
and $K_\theta = \cos(\varphi_1 - \theta_1)$ = displacement factor

$PF = Current\ distortion\ factor \cdot Displacement\ factor$

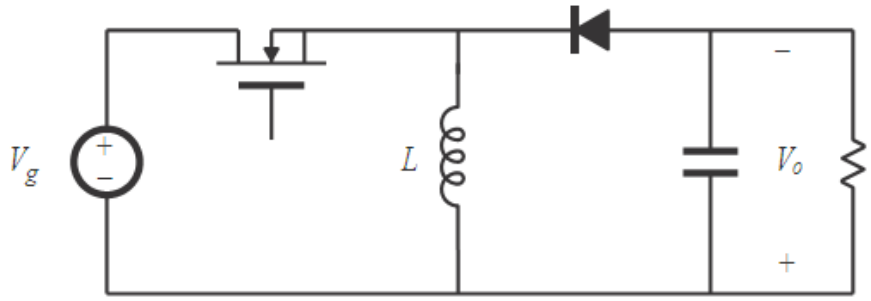
2. *The four basic dc-dc nonisolated converters: buck, boost, buck-boost, Ćuk: schematics with practical semiconductors and their static conversion ratios values.*



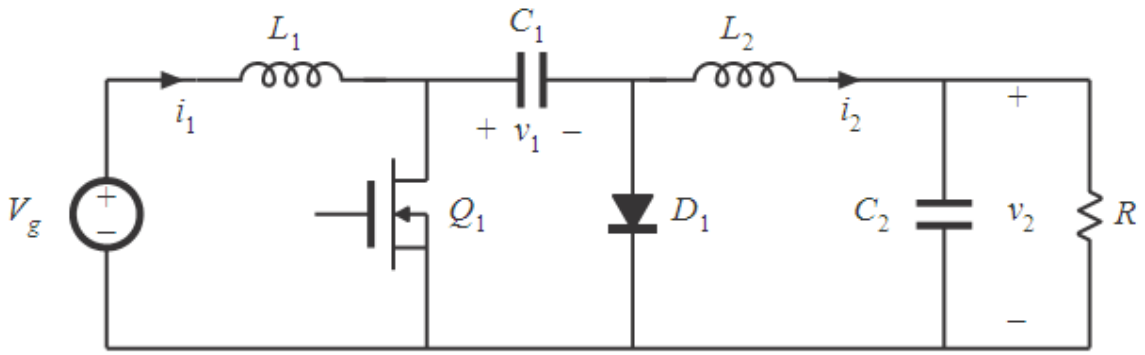
Buck converter. $M(D) = D$



Boost converter. $M(D) = \dfrac{1}{1-D}$

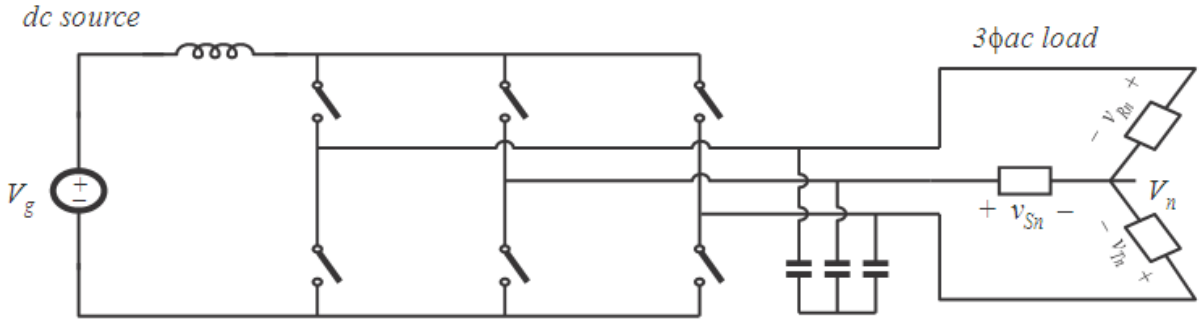


Buck-Boost converter. $M(D) = \dfrac{D}{1-D}$

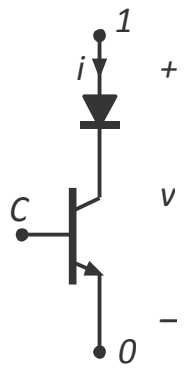


Ćuk converter. $M(D) = \dfrac{D}{1-D}$

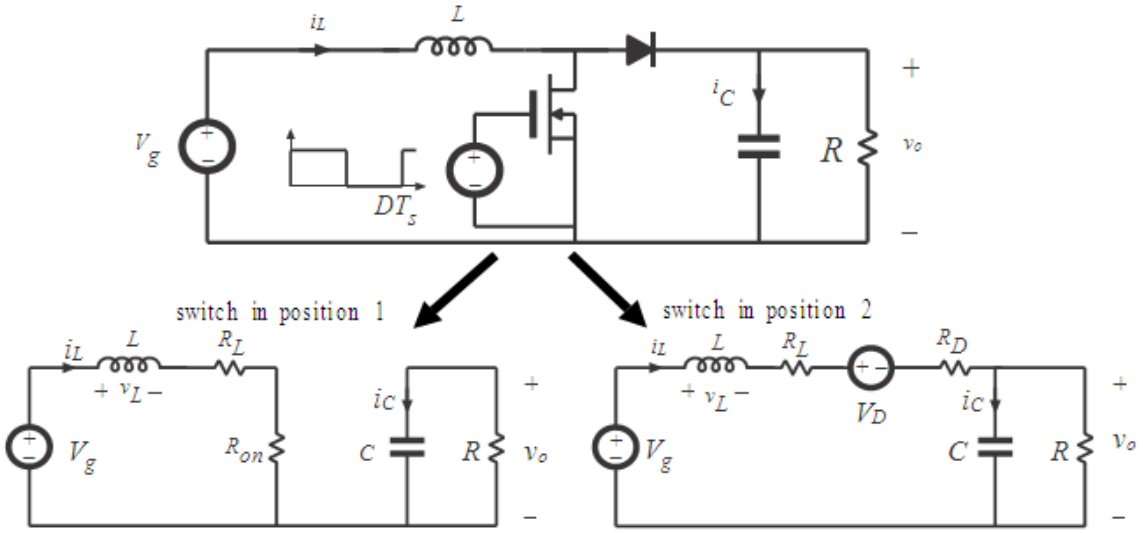
3. The three phase current source inverter – schematics, characteristic nature, switch implementation.



Exhibits a *boost-type* conversion characteristic. The switches are current unidirectional (voltage bidirectional) two quadrant switches, such as:



4. ***Nonideal converters analysis. Literally calculate the static conversion ratio*** M ***and efficiency*** η ***of a boost converter taking into account inductor series resistance*** R_L ***and semiconductor conduction losses: transistor on resistance*** R_{on} ***and diode forward voltage drop*** V_D***. Use small ripple assumption together with volt-second balance and charge balance equations. At what duty cycles efficiency becomes poor when only transistor conduction losses are taken into account?***



Small-ripple assumption: inductor current i_L and capacitor voltage v_o have negligible ripple and therefore they may be assumed as constant, denoted by capitals, I_L, V_o.

Volt- second balance equation:

$$D(V_g - I_L R_L - I_L R_{on}) + (1-D)(V_g - I_L R_L - V_D - I_L R_D - V_o) = 0 \qquad (1)$$

Charge balance equation:

$$D\left(-\frac{V_o}{R}\right) + (1-D)\left(I_L - \frac{V_o}{R}\right) = 0 \qquad (2)$$

Equations (1) and (2) together are a linear system with I_L and V_o as unknowns.

Solve for *M*. Final result is:

$$M = \frac{1}{1-D} \cdot \frac{1-\frac{V_D}{V_g}}{1+\frac{1}{(1-D)^2}\cdot\frac{R_L}{R}+\frac{D}{(1-D)^2}\cdot\frac{R_{on}}{R}+\frac{1}{1-D}\cdot\frac{R_D}{R}} \tag{3}$$

Now efficiency can be estimated as output to input average powers ratio:

$$\eta = \frac{P_o}{P_g} = \frac{\frac{V_0^2}{R}}{V_g I_L} \tag{4}$$

On the other side, from (2) $I_L = \frac{V_0}{R(1-D)}$ and substituting in (4) one obtains:

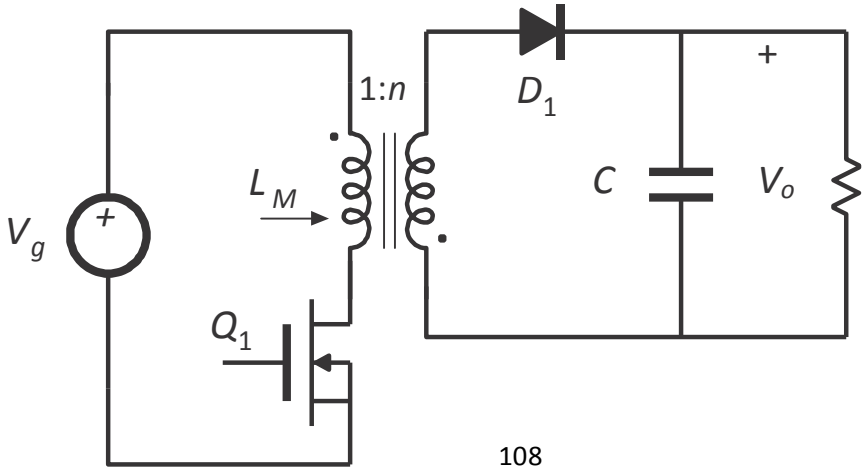
$$\eta = (1-D)\frac{V_o}{V_g} = (1-D)M \overset{(1)}{=} \frac{1-\frac{V_D}{V_g}}{1+\frac{1}{(1-D)^2}\cdot\frac{R_L}{R}+\frac{D}{(1-D)^2}\cdot\frac{R_{on}}{R}+\frac{1}{1-D}\cdot\frac{R_D}{R}} \tag{5}$$

When only transistor conduction losses are taken into account efficiency formula form (5) becomes ($R_L = R_D = 0$, $V_D = 0$):

$$\eta = \frac{1}{1+\frac{D}{(1-D)^2}\cdot\frac{R_{on}}{R}} = \eta(D) \tag{6}$$

As $\eta(0) = 1$ and $\lim\limits_{\substack{D\to 1\\ D<1}} \eta(D) = 0$ it is clear that efficiency becomes poor at high duty cycles.

5. *The flyback converter: schematics, static conversion ratio, applications, advantages and limitations.*



$$M(D) = n\frac{D}{1-D} = n\frac{D}{D'}$$

- ✓ Widely used in low power and/or high voltage applications
- ✓ Low parts count
- ✓ Multiple outputs are easily obtained, with minimum additional parts
- ✓ Often operated in discontinuous conduction mode
- ✓ Cross regulation is inferior to buck-derived isolated converters

6. *The classical single-transistor forward converter: schematics, main waveforms, maximum duty cycle.*

From magnetizing current volt-second balance

$$DV_g + (D_2)(-\frac{n_1}{n_2}V_g) + D_3 \cdot 0 = 0$$

Solve for D_2:

$$D_2 = \frac{n_2}{n_1}D$$

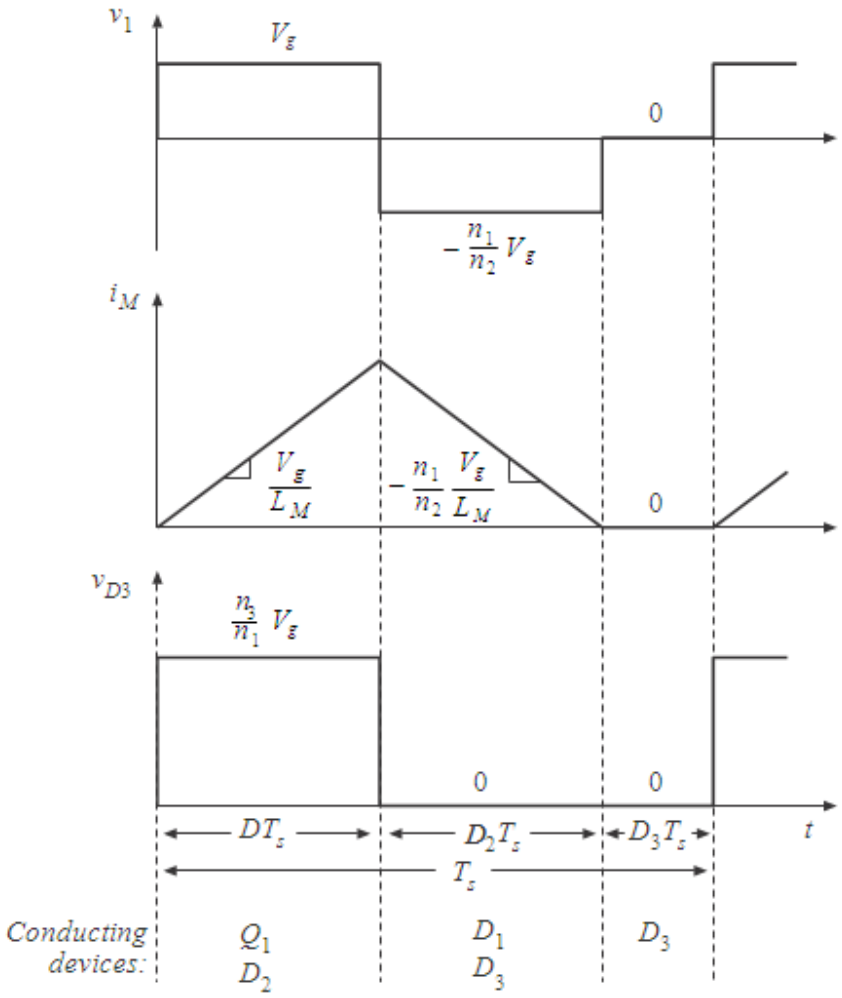
D_3 cannot be negative. But $D_3 = 1 - D_2 - D$. Hence, using the value for D_2 previously obtained, it follows that:

$$1 - \frac{n_2}{n_1}D - D \geq 0\,,$$

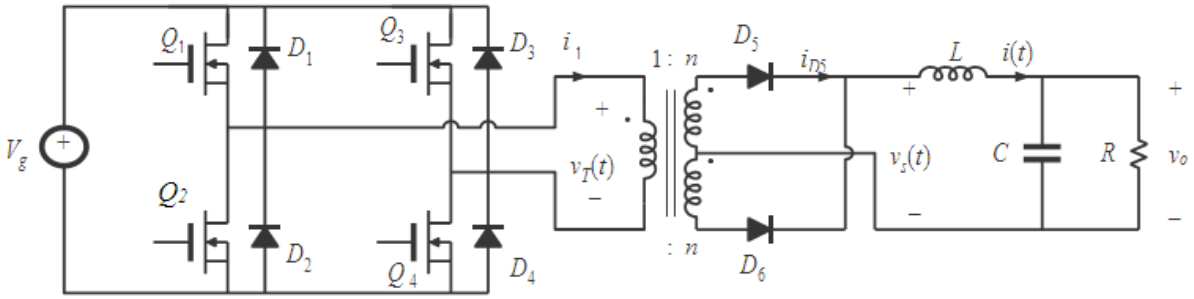
finally resulting in

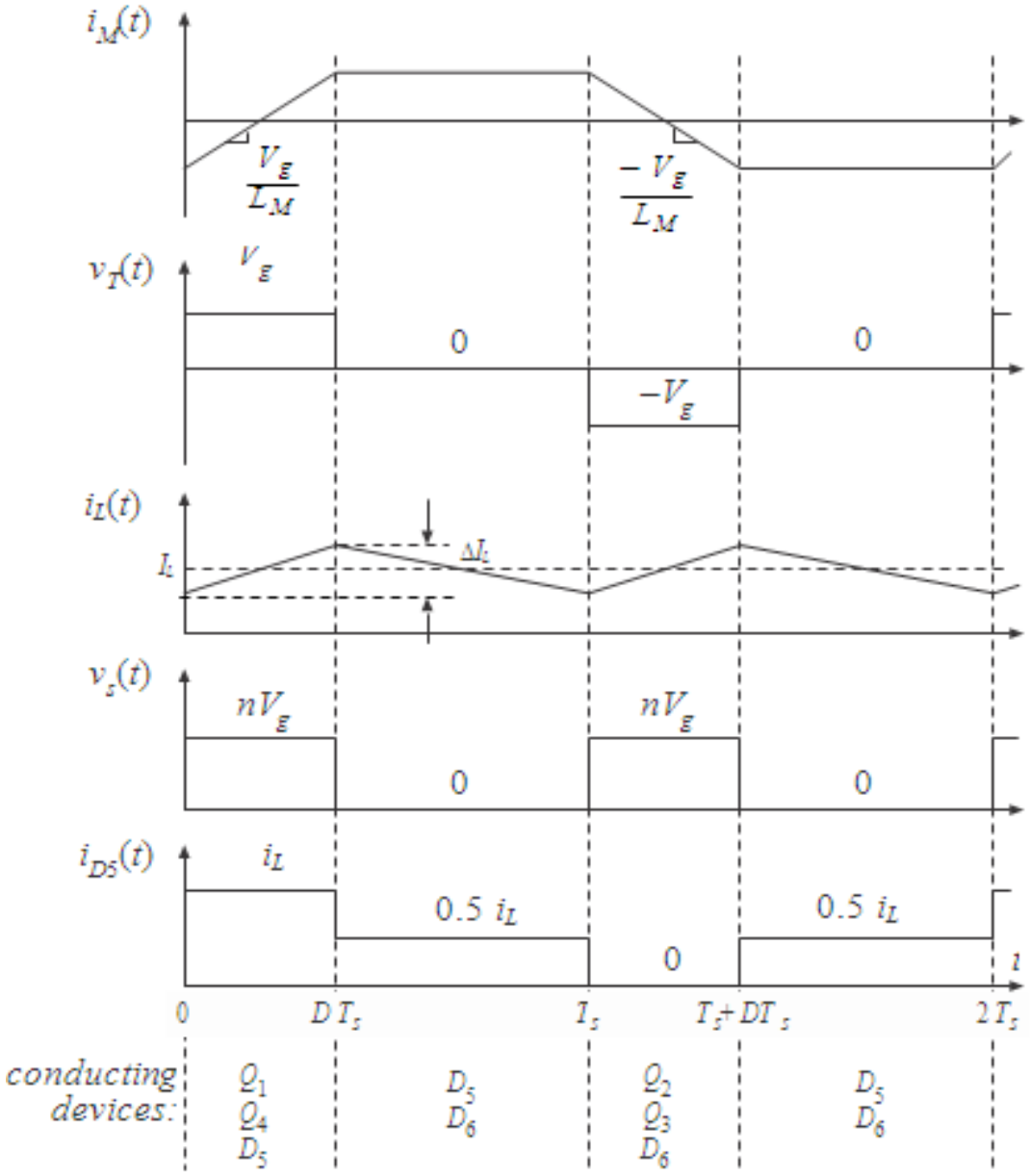
$$D \leq \frac{1}{1+\frac{n_2}{n_1}}$$

If the final result is provided without proof the anwer will also be accepted.



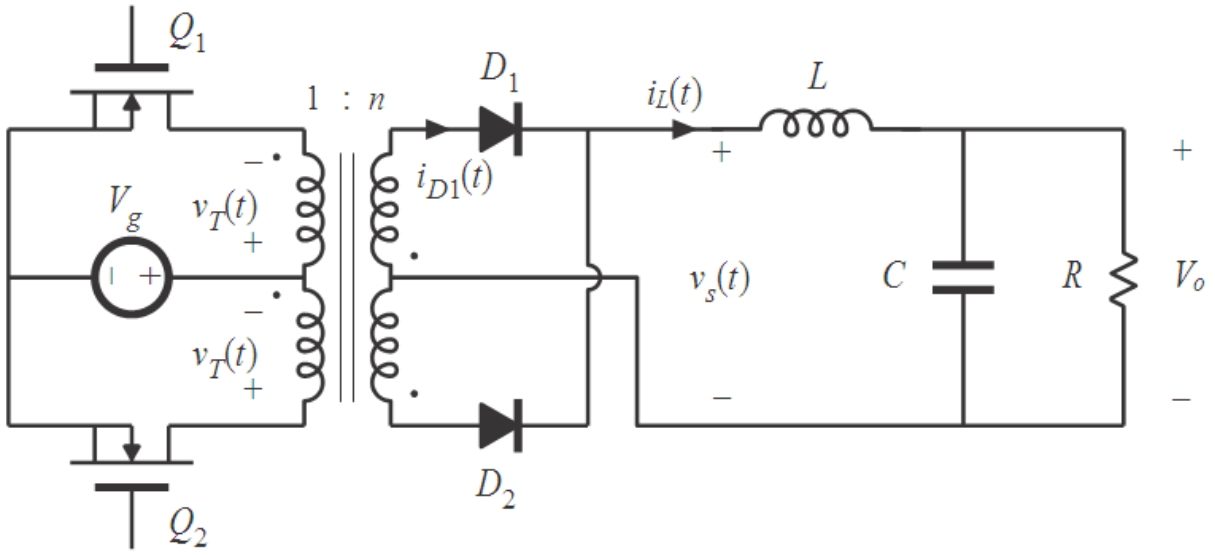
7. The full-bridge isolated buck converter: schematics, main waveforms, solutions for preventing core saturation.





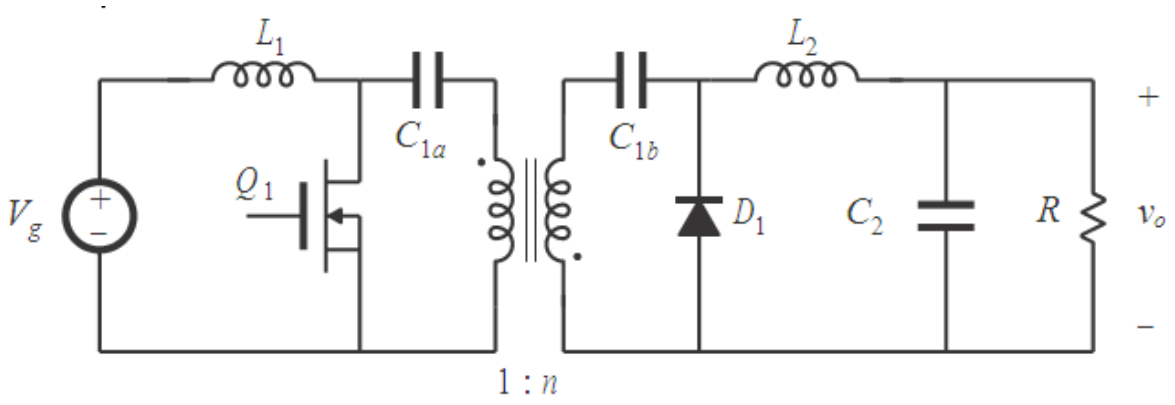
Saturation can be prevented by placing a *capacitor* in series with primary or by use of the so called *current programmed mode.*

8. *Push-pull isolated buck and isolated Ćuk converters: schematics, type of control, advantages and disadvantages regarding transformer magnetizing current.*



Push-pull isolated buck-derived converter

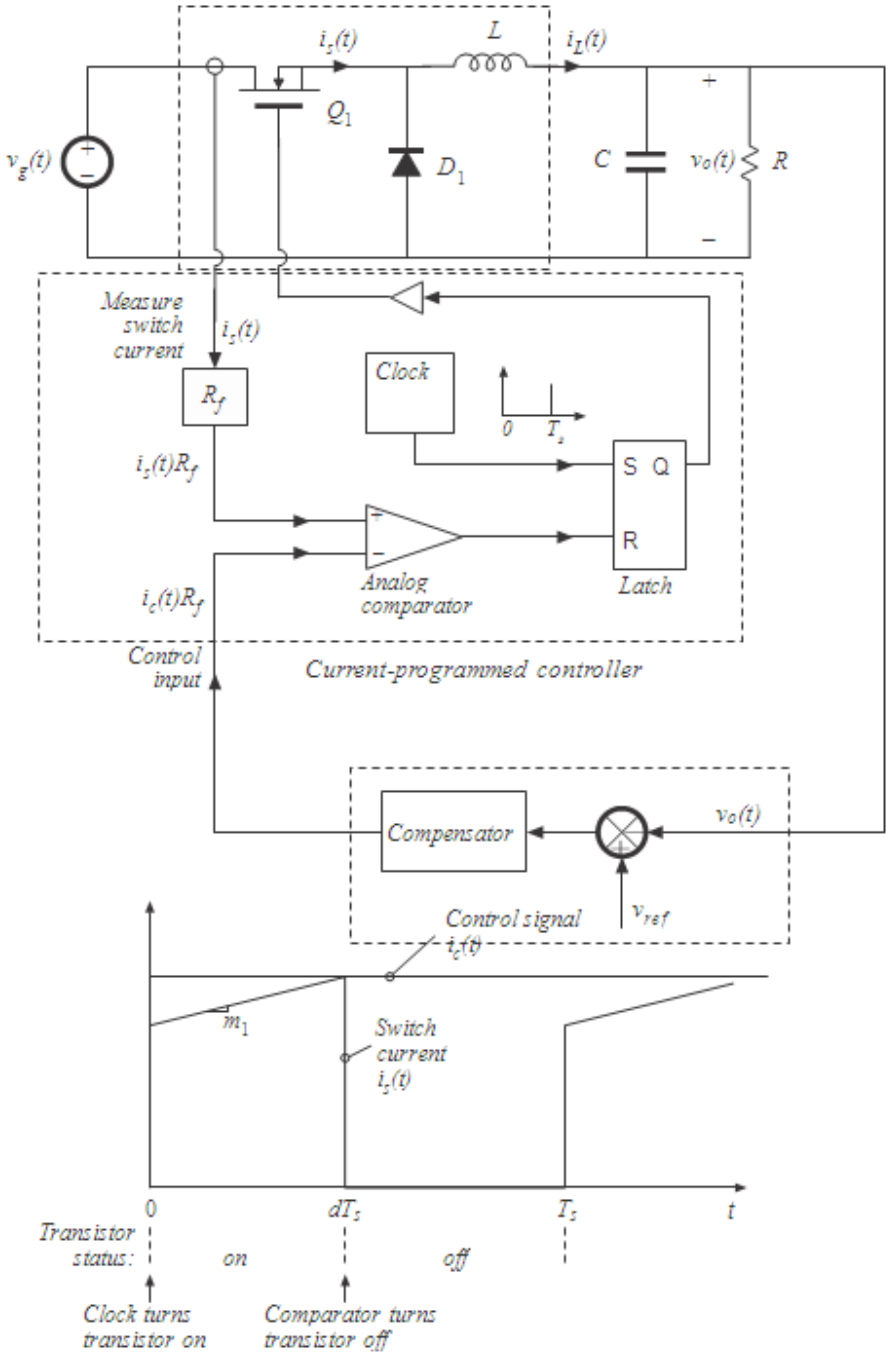
Current programmed control can be used to mitigate transformer saturation problems. Duty cycle control not recommended.



Ćuk isolated buck-derived converter

Capacitors C1a, C1b ensure that no dc voltage is applied to transformer primary or secondary windings. Transformer operates in conventional manner, with small magnetizing current and negligible energy storage within the magnetizing inductance.

9. Current programmed control principle (for a buck converter): block diagram, advantages, disadvantage, stability.



Advantages:

- ✓ Simpler dynamics —inductor pole is moved to high frequency.
- ✓ Simple robust output voltage control, with large phase margin, can be obtained without use of compensator lead networks.

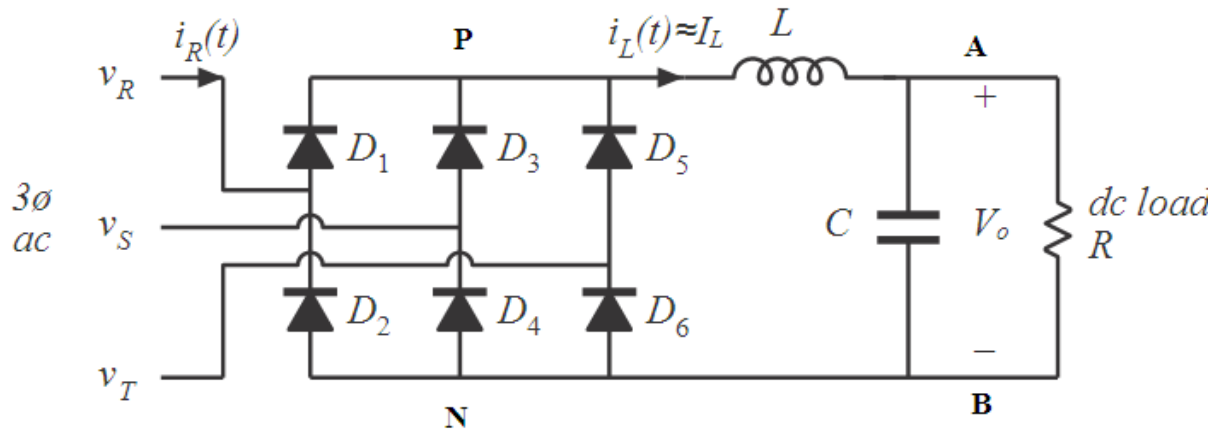
✓ Transistor failures due to excessive current can be prevented simply by limiting $i_c(t)$.

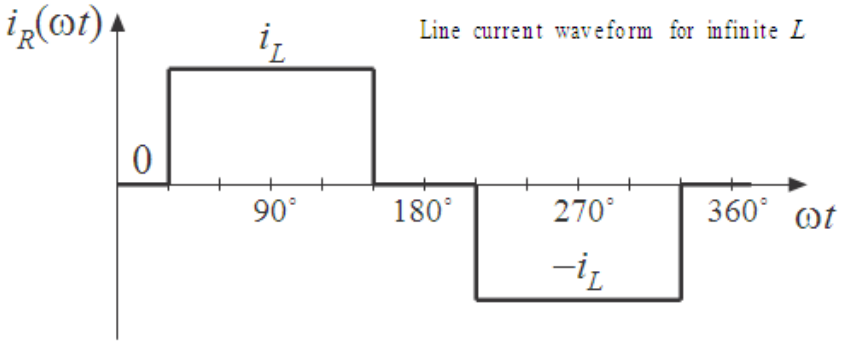
✓ Transformer saturation problems in bridge or push-pull converters can be mitigated.

Disadvantage: susceptibility to noise, instability problems.

The current programmed controller is inherently unstable for $D > 0.5$, regardless of the converter topology. Controller can be stabilized by addition of an artificial ramp.

10. The three-phase bridge rectifier (six pulse rectifier): schematics, line current for high load inductor, harmonic content of the line current and output voltage.





✓ Dc and a fundamental of *six* times the line frequency in the output voltage. That is the harmonics, relative to line frequency are: 0, 6, 12, 18, etc.

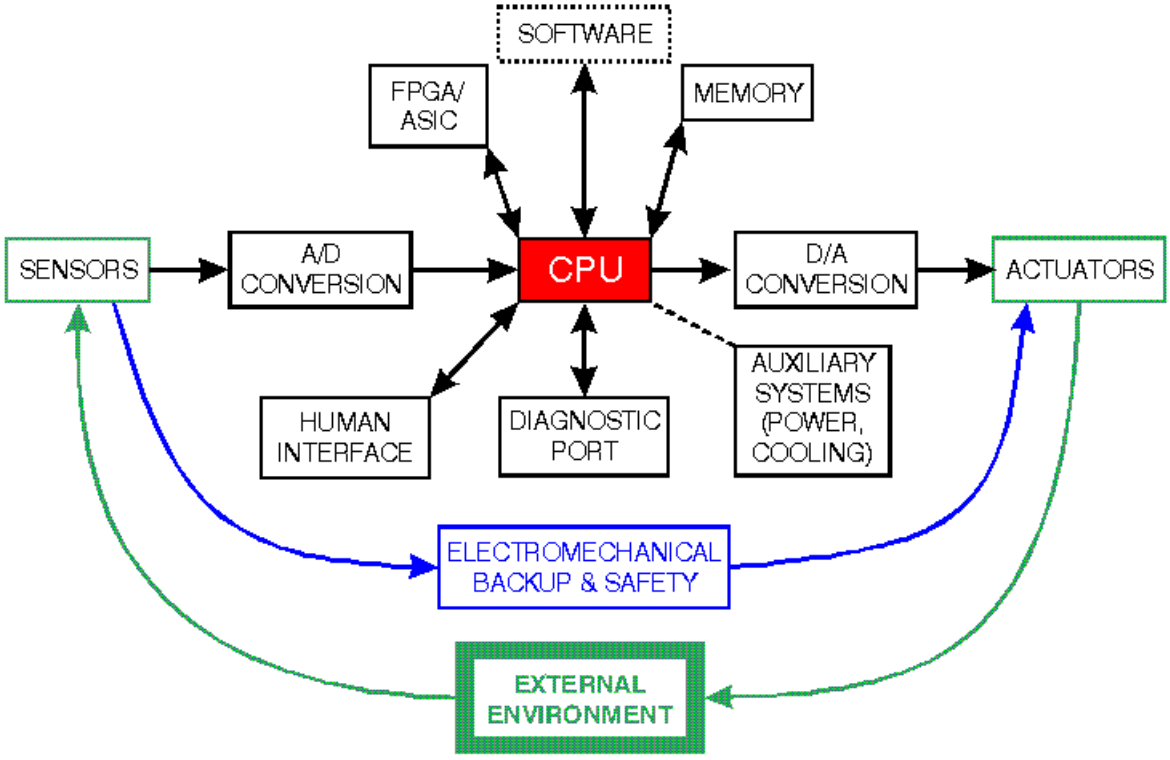
✓ Odd non-triplen harmonics in the ac line current.

Embedded Systems

1. *The general architecture of an embedded system.*

Answer: C.-D. Căleanu, Embedded Systems. Course Notes, 2011

https://intranet.etc.upt.ro/~EMBEDDED_SYS/Course , CHAPTER 1 slide 21.



2. *What are the relative advantages/disadvantages of RISC versus CISC architectures?*

Answer: C.-D. Căleanu, Embedded Systems. Course Notes, 2011

https://intranet.etc.upt.ro/~EMBEDDED_SYS/Course , CHAPTER 3, slides 13-15.

- The most common types of general-purpose ISA architectures implemented in embedded processors are:
- Complex Instruction Set Computing (CISC) Model
- Reduced Instruction Set Computing (RISC) Model

Complex Instruction Set Computing (CISC) Characteristics:

- A large number of instructions each carrying out different permutation of the same operation
- Instructions provide for complex operations
- Different instructions of different format
- Different instructions of different length
- Different addressing modes
- Requires multiple cycles for execution

Reduced Instruction Set Computing (RISC) Characteristics:

- Fewer instructions aiming simple operations that can be executed in a single cycle
- Each instruction of fixed length – facilitates instruction pipelining
- Large general purpose register set – can contain data or address
- Load-store Architecture – no memory access for data processing instructions

3. Enounce and explain the role of the following ARM registers: r13, r14 and r15, status registers.

Answer: C.-D. Căleanu, Embedded Systems. Course Notes, 2011

https://intranet.etc.upt.ro/~EMBEDDED_SYS/Course , CHAPTER 4, slide 17, 21

Three registers r13, r14, r15 perform special functions:

r13 – stack pointer,

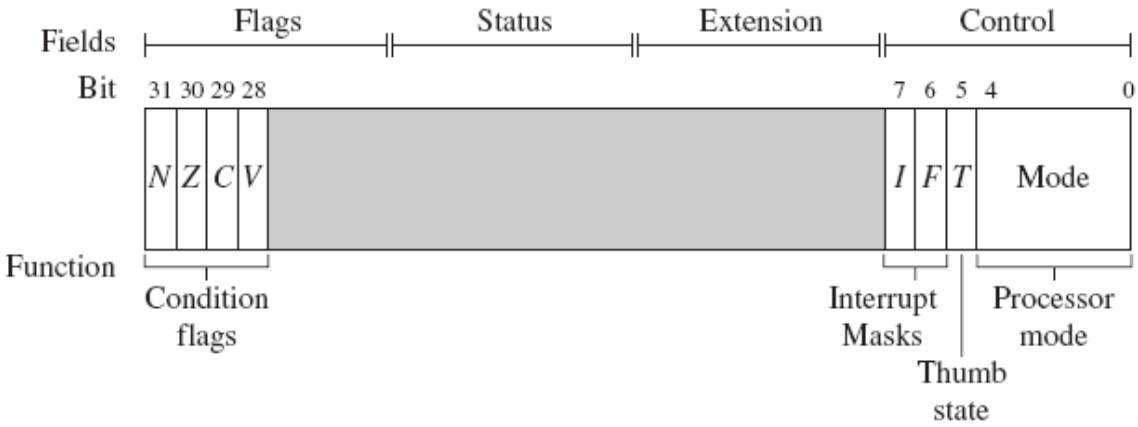
r14 – link register where return address is put whenever a subroutine is called,

r15 – program counter

In addition, there are two status registers

- CPSR: current program status register
- SPSR: saved program status register

CPSR: monitors and control internal operations



The top four bits of the CPSR contain the condition codes which are set by the CPU. The condition codes report the result status of a data processing operation. From the condition codes you can tell if a data processing instruction generated a negative, zero, carry or overflow result.

The lowest eight bits in the CPSR contain flags which may be set or clear ed by the application code. Bits 7 and 8 are the I and F bits. These bits are used to enable and disable the two interrupt sources which are external to the ARM7 CPU. Most peripherals are connected to these two interrupt lines. You should be careful when programming these two bits because in order to disable either interrupt source the bit must be set to '1' not '0' as you might expect. Bit 5 is the THUMB bit.

4. *Which is the role of the barrel shifter? Present its block diagram and enumerate the basic operations which could be performed with it. Illustrate the concept with an assembly language example.*

Answer: C.-D. Căleanu, Embedded Systems. Course Notes, 2011

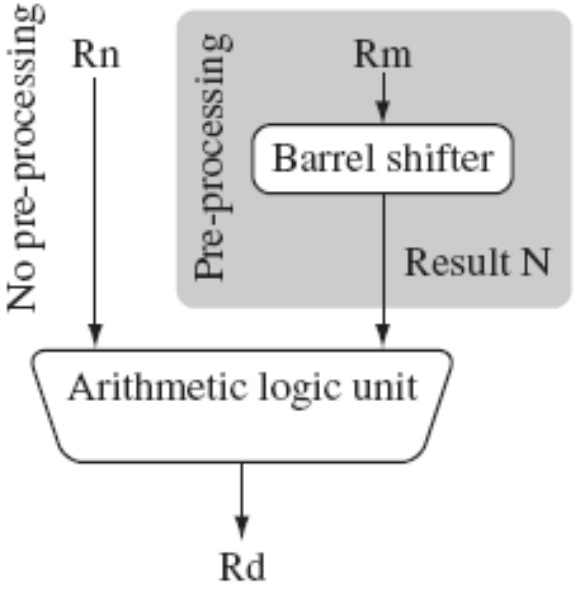
https://intranet.etc.upt.ro/~EMBEDDED_SYS/Course , CHAPTER 4, slide 43, 44.

Enables shifting 32-bit operand in one of the source registers left or right by a specific number of positions within the cycle time of instruction

Basic Barrel shifter operations: Shift left, right, rotate

Facilitates fast multiply, division and increases code density

Example: mov r7, r5, LSL #2 - Multiplies content of r5 by 4 and puts result in r7



5. Present possible implementations for the non-volatile memory. What could be store in it?

Answer: C.-D. Căleanu, Embedded Systems. Course Notes, 2011

https://intranet.etc.upt.ro/~EMBEDDED_SYS/Course , CHAPTER 5, slide 10-12.

- Mask ROM
  - Used for dedicated functionality
  - Contents fixed at IC fab time (truly write once!)
- ERPOM (erase programmable)
  - Requires special IC process (floating gate technology)
  - Writing is slower than RAM, EPROM uses special programming system to provide special voltages and timing
  - Reading can be made fairly fast
  - Rewriting is slow
    - Erasure is first required, EPROM – UV light exposure, EEPROM – electrically erasable
- Flash
  - Uses single transistor per bit (EEPROM employs two transistors)
  - A flash memory provides high density storage with speed marginally less than that of SRAM's
  - Write time is significantly higher compared to DRAM

- On-chip non-volatile storage is used for storage of:
  - Configuration information
  - Executable code that runs on core processors
  - Recorded data: repeated write

6. The I2C protocol (features, connections, advantages, disadvantages).

Answer: C.-D. Căleanu, Embedded Systems. Course Notes, 2011

https://intranet.etc.upt.ro/~EMBEDDED_SYS/Course , CHAPTER 6, slide 21, 22, 25.

I2C Features:

- Bi-directional
  - Data can flow in both directions
- Synchronous (2 wires)
  - Data is clocked along with a clock signal
  - Clock signal controls when data is changed and when it should be read. Clock rate can vary unlike asynchronous (RS-232 style) communication
- I2C bus has three speeds:
  - Slow (under 100 Kbps)
  - Fast (400 Kbps)
  - High-speed (3.4 Mbps) – I2C v.2.0

I2C Connections:

- Two wired bus
  - Serial DAta (SDA) line
  - Serial CLock (SCL) line
- Voltage Levels
  - High -1
  - Low - 0
- Bit transfer
  - SCL = 1 implies SDA = valid data
  - Stable data during high clock
  - Data change during low clocks

I2C Tradeoffs:

- Advantages:
  - Good for communication with on-board devices that are accessed occasionally
  - Easy to link multiple devices because of addressing scheme

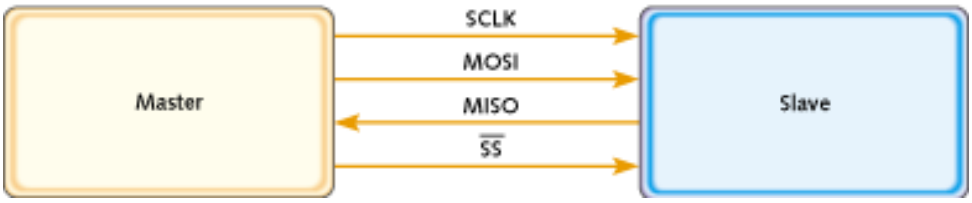
  - Cost and complexity do not scale up with the number of devices
- Disadvantages:
  - The complexity of supporting software components can be higher than that of competing schemes (for example, SPI)

7. The SPI protocol (bus configuration, comparison with I2C).

Answer: C.-D. Căleanu, Embedded Systems. Course Notes, 2011

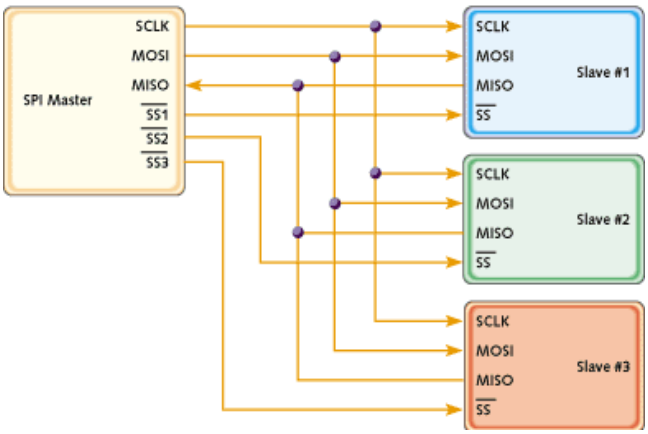
https://intranet.etc.upt.ro/~EMBEDDED_SYS/Course , CHAPTER 6, slide 27, 28.

SPI Bus Configuration



- Synchronous serial data link operating at full duplex
- Master/slave relationship
- 2 data signals:
  - MOSI – master data output, slave data input
  - MISO – master data input, slave data output
- 2 control signals:
  - SCLK – clock
  - /SS – slave select (no addressing)

SPI vs. I^2C



- For point-to-point, SPI is simple and efficient
  - Less overhead than I2C due to lack of addressing, plus SPI is full duplex.
- For multiple slaves, each slave needs separate slave select signal
  - More effort and more hardware than I2C

8. Enumerate the functions of the start-up code.

Answer: C.-D. Căleanu, Embedded Systems. Course Notes, 2011

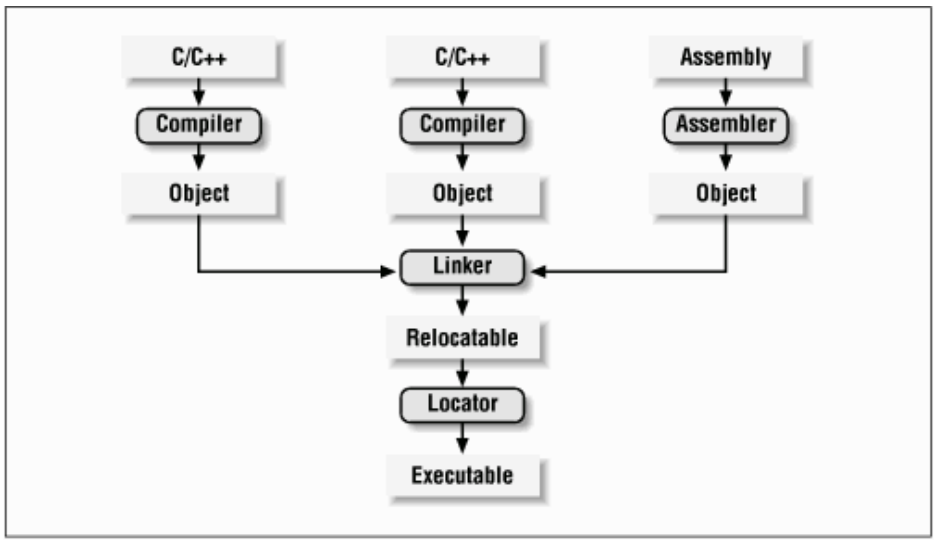
https://intranet.etc.upt.ro/~EMBEDDED_SYS/Course , CHAPTER 7, slide 20.

- Start-up code usually consists of the following actions in sequence:
  - Disable all interrupts
  - Copy any predefined data from ROM to RAM
  - Zero the uninitialized data area
  - Allocate space and initialize the stack
  - Initialize processor's SP
  - Create and initialize the heap
  - Possibly execute constructors and initializers for global variables for object oriented languages like C++
  - Enable interrupts
  - Call main

9. Enounce the typical steps involved in the software building process.

Answer: C.-D. Căleanu, Embedded Systems. Course Notes, 2011

https://intranet.etc.upt.ro/~EMBEDDED_SYS/Course , CH. 7, slide 25.



10. Define the kernel and its responsibilities.

Answer: C.-D. Căleanu, Embedded Systems. Course Notes, 2011

https://intranet.etc.upt.ro/~EMBEDDED_SYS/Course , CH. 8, slide 12, 13.

Kernel's definition

- Most frequently used portion of OS
- Resides permanently in main memory
- Runs in privileged mode
- Responds to calls from processes and interrupts from devices

Kernel's responsibility

- Managing Processes
- Context switching: alternating between the different processes or tasks
    - Various scheduling algorithms
    - Scheduling: deciding which task/process to run next
- Various solutions to dealing with critical sections
    - Critical sections = providing adequate memory-protection when multiple tasks/processes run concurrently

Electronic Equipment Testing

1. *Test levels: definition and description of each level's characteristics*

There are three levels of test:

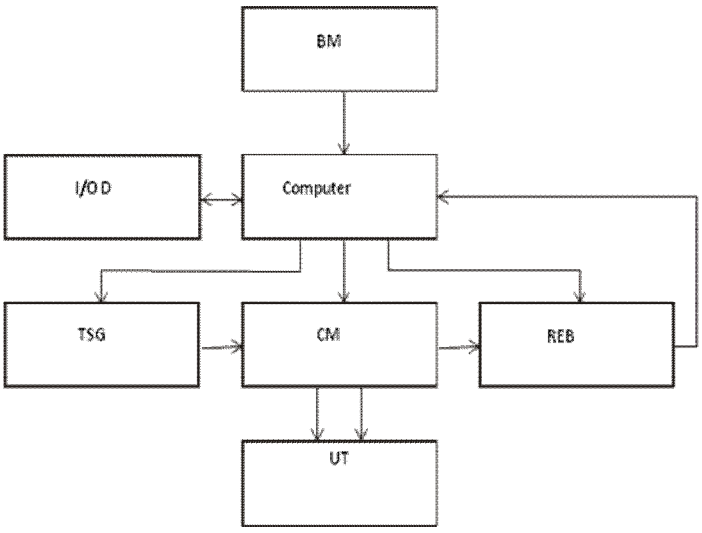
- electronic component (including printed circuit board),
- equipped electronic board (mounted components),
- equipment.

a) failed test at the component level – the component should not be mounted on the board, economically has been proven that this test (also done by the producer) should be repeated by the user

b) can be done through "nail bed testing" (complicated and costly for realizing the test equipment) or through "test stimulus generation" (simple connection, but costly for implementing the test program)

c) depends on the equipment: normally involves broken connections between functionally correct boards. Can involve some more sophisticated equipment, such as the signature analyzer.

2. *Architecture of an automatic test equipment. Characteristics of each block's functionality*



UT – unit under test

TSG – test signal generator

REB – responses evaluation block

CM – connection matrix

BM – back-up memory

3. Principles of the signature analyzer

The signature analyzer is based on the principle of data information flow compression. The long data sequences are acquired from the tested board/equipment and compressed into fixed-length information, called "signature". The signature should be easy to be recognized, easy to be interpreted by comparing it with a control signature that corresponds to the correct functioning.

According to how the data flow is collected, the signature analyzer can be: serial or parallel.

The heart of the signature analyzer is a Pseudo-Random Sequence Generator, that performs data compression. The signature is provided as a fixed length information, on 16 bits, decoded into groups of 4 bits, displayed as alphanumeric characters on 7 segment LEDs. It avoids using small alphabet letters (b, c, d) and ambiguous capital letters (B, D, G, I), using instead letters like H, P, T, U.

The signature should be simple to be recognized, un-ambiguous and stable.

The signature analyzer should have the auto-test facility, in order to avoid wrong decisions.

4. Principles of testing the static parameters of a digital integrated circuit

The static parameters of an IC are:

- Input and output voltages
- Input and output currents

They are stable during the test. A time should be given from powering the IC, in order to allow stabilisation of the transition factors.

Test should be carried out under the less favourable conditions: minimum power supply value, maximum circuit's charge, etc.

The Test Signal Generator is formed by a number of Programmable Voltage Sources (PVS) and Programmable Constant Current Generators (PCCG).

The Responses Evaluation Block is a simple measuring instrument.

The Connection Matrix is formed by a number of relays or commuting transistors.

5. *Principles of testing the dynamic parameters of a digital integrated circuit*

The dynamic parameters of an IC are:

- the transition times: t_{tLH}, t_{tHL}
- the propagation times: t_{pLH}, t_{pHL}

Those parameters might be defined by fixed or percentage thresholds. The realisation of the testing structure depends on that definition.

The evaluation should be done in the worst functional case: power supply, charge, etc

The Test Signal Generator uses digital programmable pulse generators: fronts, length, amplitude, polarity, filling factor, etc

The Responses Evaluation Block is typically formed by a counter, with "start" and "stop" commanded by the discriminated fronts of the tested parameter.

6. *Principles of the modular activation method for processors' functional tests*

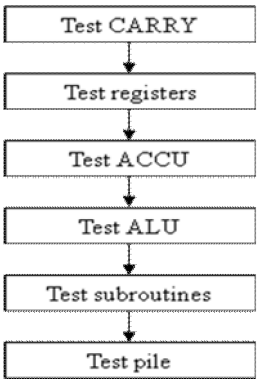
The processor is divided on hierarchical levels (both functional and hardware).

The test is done based on a self-test program.

The program starts with the basic level

Each tested level can be used for testing superior levels

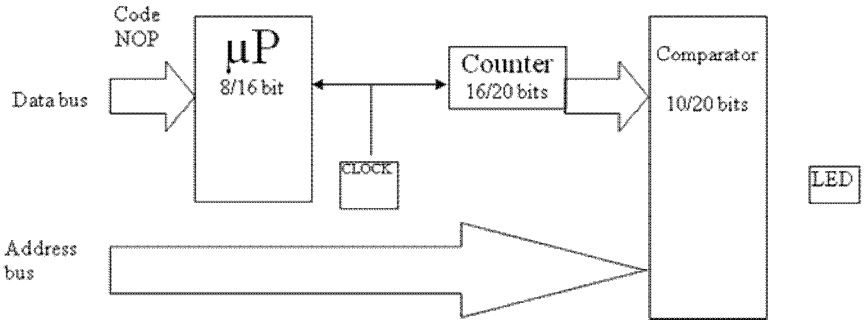
A possible testing strategy:



In order to start, a minimum level of components and functions should be correct! - KERNEL

The kernel should include: initialization circuits, program counter, address bus, data bus, instruction decoder, clock circuit

The hardware test of the kernel might be done through the following strategy:



If the kernel test is passed, the following circuits are functionally corrects:

- Clock circuit
- Initialization circuit
- Program counter
- Address bus
- Data bus – partially
- Instruction decoder – partially
- Instruction register – partially

7. ***Principles of the test stimulus vectors' generation***

The test stimulus vectors are generated through algorithms that are describing the functions of the schema on a digital electronic board.

The main methods used are:

- Single Path Activation Method
- Poage
- Poage McCluskey

There are two basical principles:

- forcing the complement of the tested error into the test node, then activation the propagation of the value in that node towards the observable output, where the received value is compared in order to take the decision: correct or erroneous board

- describing the functions on the board by using supplementary variables that are describing the functioning status of each line through their activation, then the condition to get complementary values at the output in case of "erroneous" or "correct" board is used in order to calculate the test stimulus vectors.

8. *Principles for testing the Bit Error Rate for a telecommunication digital network*

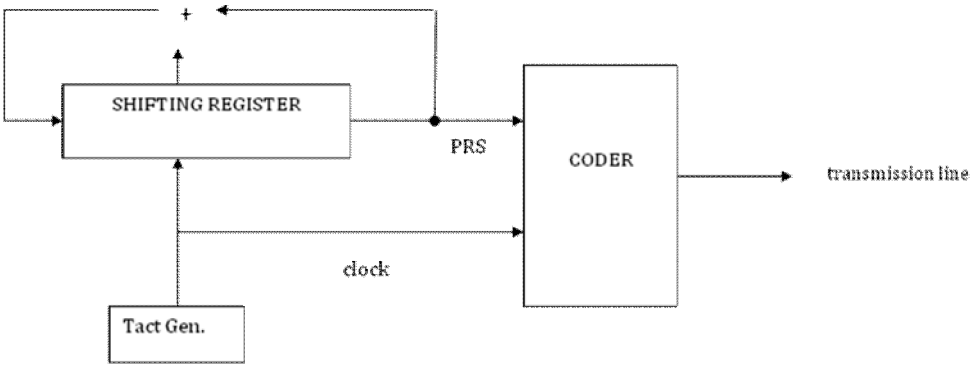
The Bit Error Rate (BER) is the ratio between the number of error bits and the total number of transmitted bits

BER estimation can be done:

- in-service
- out-of-service

The test signal is a pseudorandom binary sequence, standardized through the 0.151 CCITT recommendation.

The principle of the test generator used at the transmission end is:



The problem is: avoiding the lock on 0 of the shift register.

At the reception end, there is a similar signal generator that provides the same sequence as at the emitter end, that is compared to the one received through the telecom network.

The problem is to ensure synchronization between the two generators.

9. *Principles for the realization of a fault tolerant system*

Fault tolerance is an architectural attribute of a system, making possible for the system to function properly even when one or more faults appear in its structure.

Implementation is done through "redundancy", but the price to be paid is the high cost.

The use is in very critical applications: nuclear, military, aero-spatial, etc.

Fault = physical problem of one of the system's elements, taking to the permanent, temporary or intermittent erroneous function of the system

Error = symptom of a fault

The used strategies are:

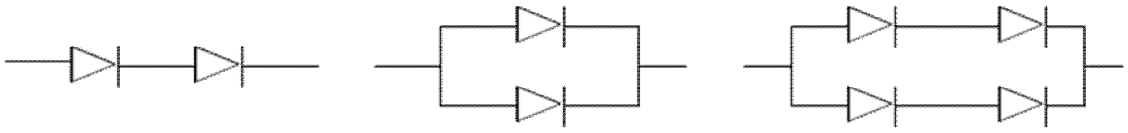
- Fault diagnosis and faulty elements replacement
- Fault masking
- Mixed strategies

The used testing methods are:

- Initial testing: before normal operation
- On-line testing: during normal operation
- Off-line testing: for error detection and diagnosis
- Redundant modules testing: in order to see if the redundant modules are able to replace the modules that have been detected as faulty

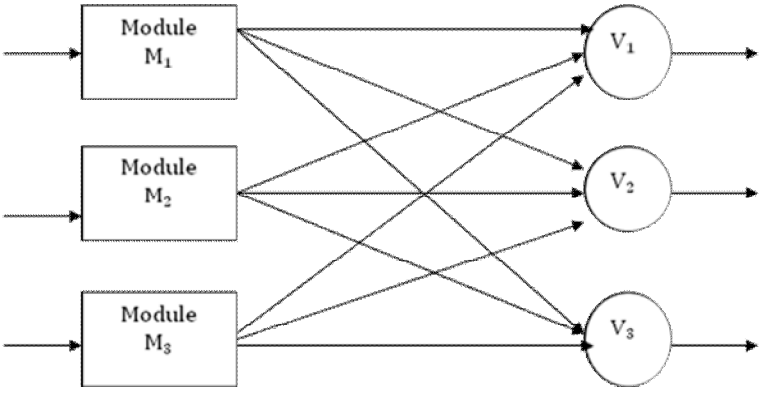
Redundancy is used in order to reconfigure the system: totally or partially.

A simple example of using redundancy in order to ensure protection to: shortcircuit, interruption, shortcircuit and interruption, respectively:

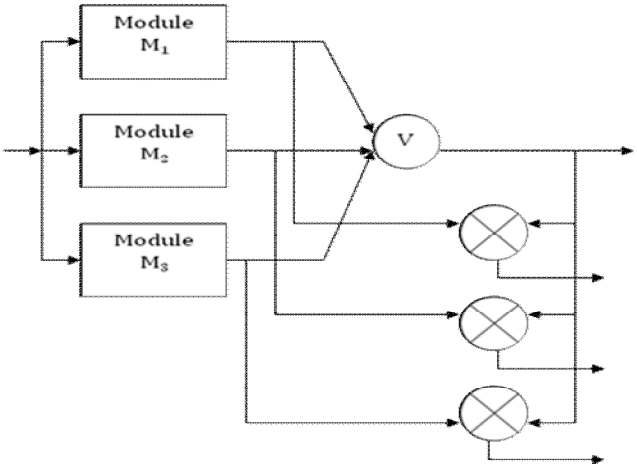


10. Principles for the detection of the faulty module in redundant electronic structures

The fault tolerant systems are implemented based on the use of majority logic redundant structures. The are using a multiple voter configuration:



In order to avoid that the error, once appeared in a module, be propagated into the system, the faulty module should be detected and replaced.



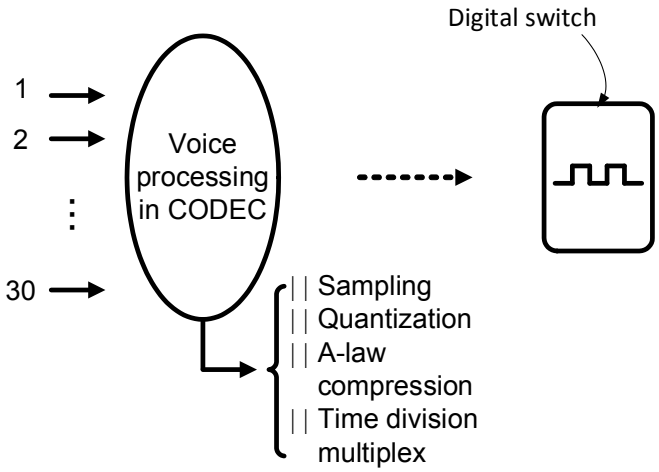
Integrated Digital Networks

1. *Compare the PCM codec solutions.*

https://intranet.etc.upt.ro/~DIG_INT_NET/course/2_Primary_PCM_CODEC.pdf, 1, 2, 4

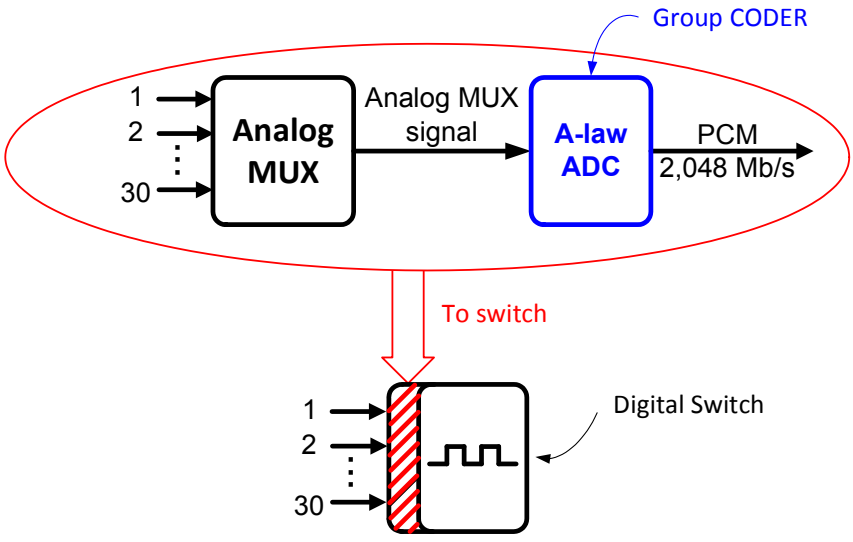
PCM CODEC

Functions



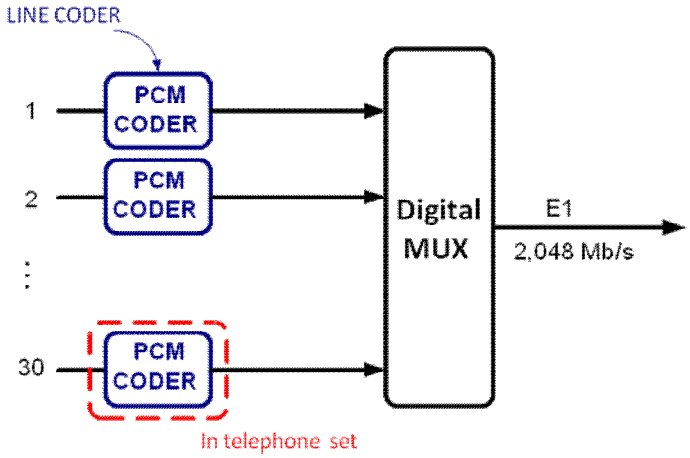
Group PCM CODEC

Solution 1



Line PCM CODEC

Solution 1



2. *Principle of positive justification.*

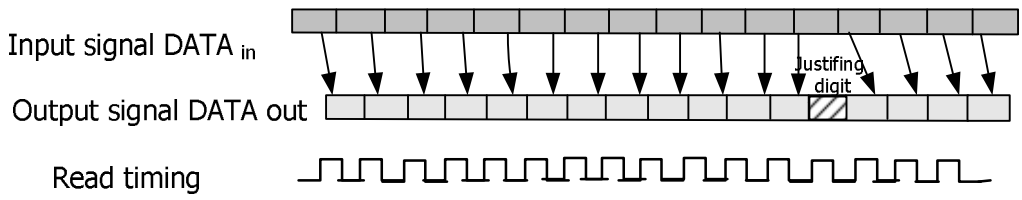
https://intranet.etc.upt.ro/~DIG_INT_NET/course/3_Secondary_Digital_TDM.pdf, 5, 7, 9

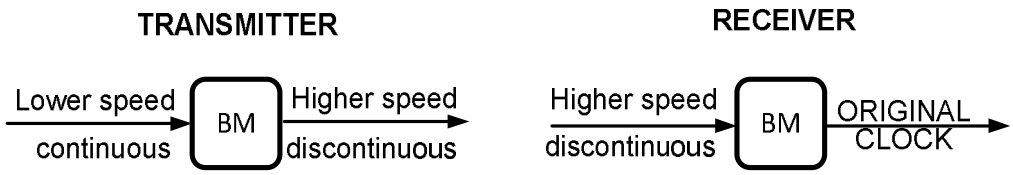
TDM secondary multiplex

Multiplexing clock frequency

$f_{TRIBUTARY\ CLOCK} < f_{SEC.\ MUX\ CLOCK}$

Principle of Positive Justification (III+V)

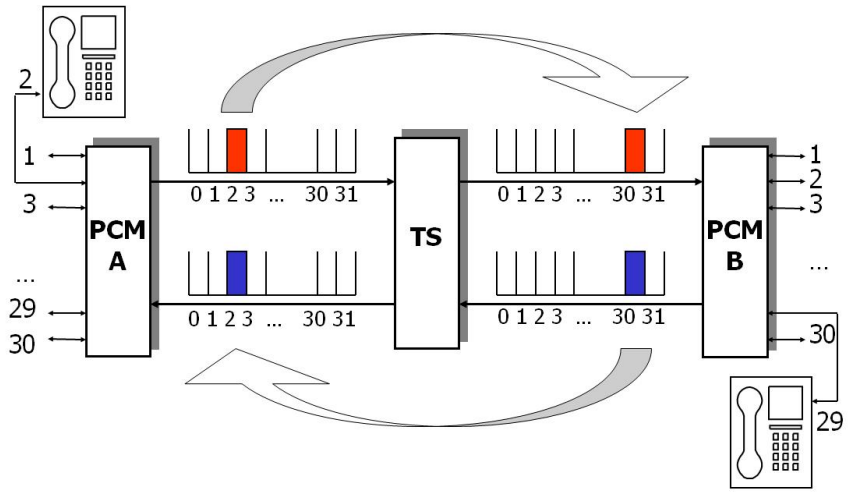




3. *Digital switching – definition, the principle of the temporal switch, the principle of the spatial switch*

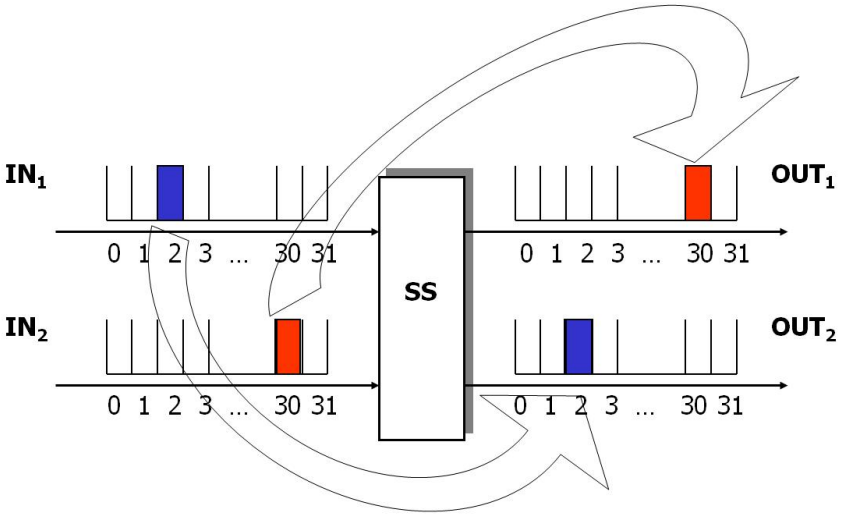
https://intranet.etc.upt.ro/~DIG_INT_NET/course/4_Digital_switching.pdf, 1, 3, 8-10

Principle of temporal switching



any TS of **any** data flow to **any** TS of the **same** data flow

Principle of spatial switching



any TS of **any** data flow to the **same** TS of **any** data flow

Digital switch

DIGITAL SWITCH

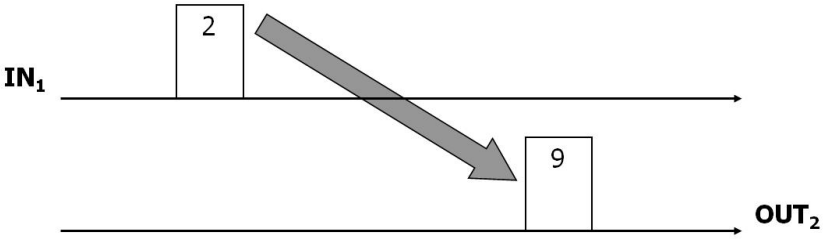
- **any** TS of **any** INPUT (data flow) to **any** TS of **any** OUTPUT (data flow)

TEMPORAL SWITCH

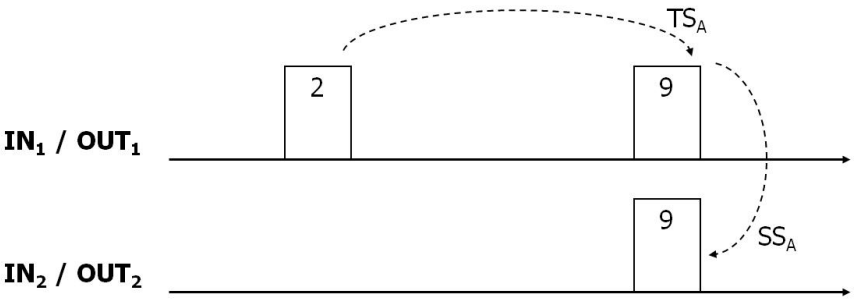
- **any** TS of **any** data flow to **any** TS of the **same** data flow

SPATIAL SWITCH

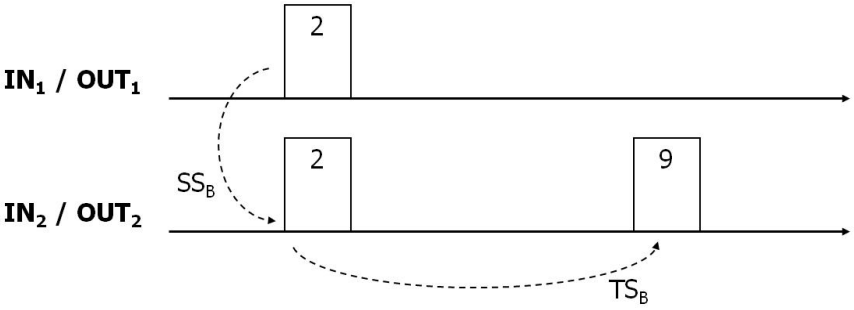
- **any** TS of **any** data flow to the **same** TS of **any** data flow



Digital switch – solution 1: TS



Digital switch – solution 2: ST

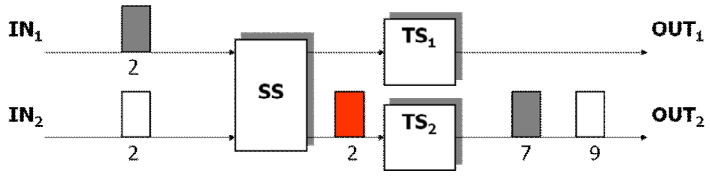


4. *Digital switch blocking – definition and example of one switch with blocking and one switch without blocking*

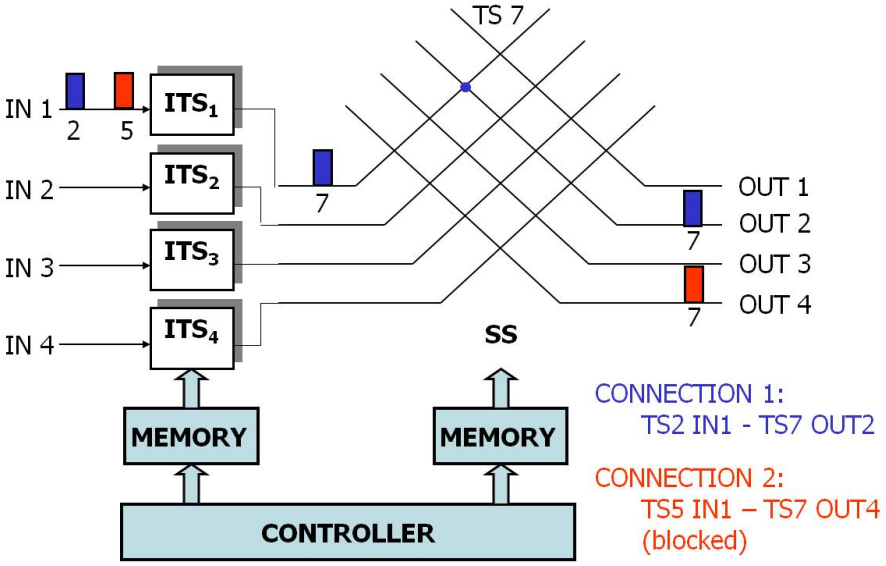
https://intranet.etc.upt.ro/~DIG_INT_NET/course/4_Digital_switching.pdf, 11-16

Blocking possibility in digital switch

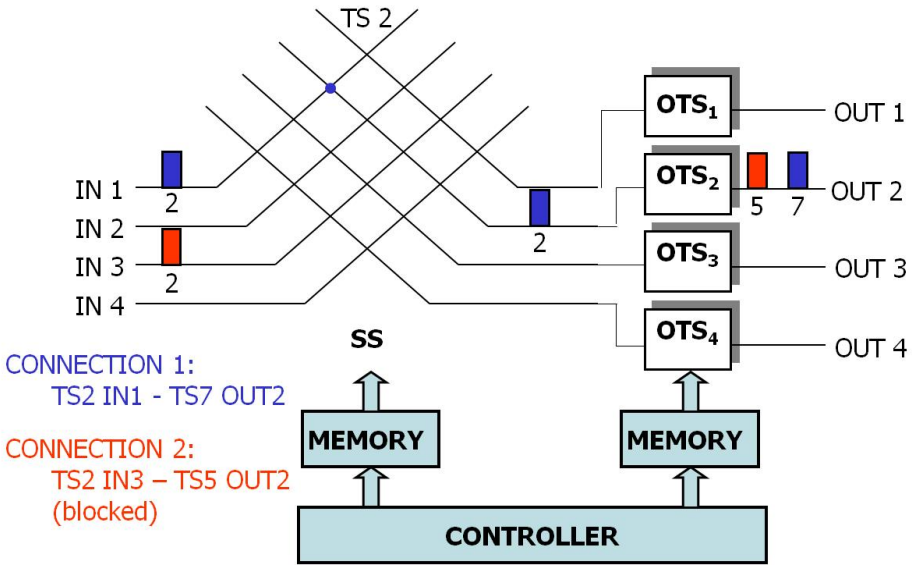
CONNECTION 1: TS2 IN1 - TS7 OUT2
CONNECTION 2: TS2 IN2 - TS9 OUT2



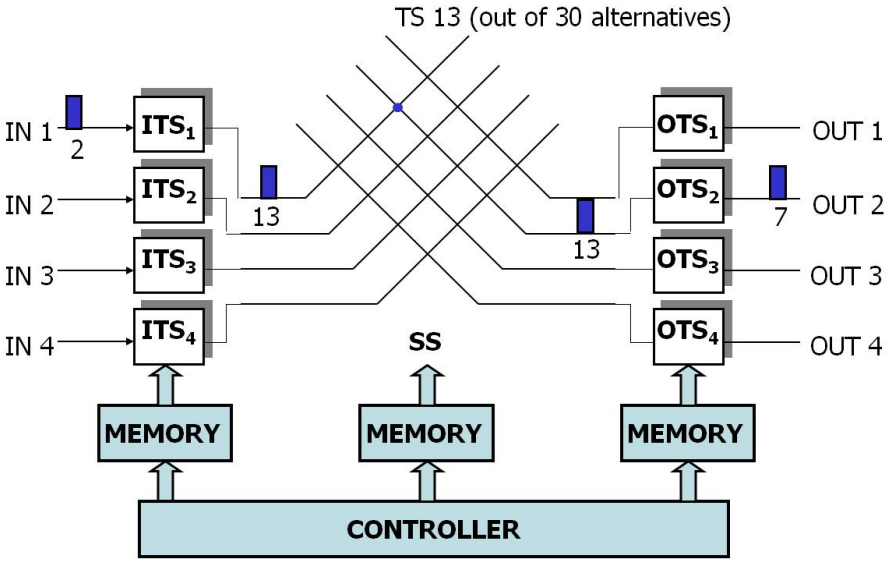
TS switch – 4 IN, 4 OUT – 120 chanels



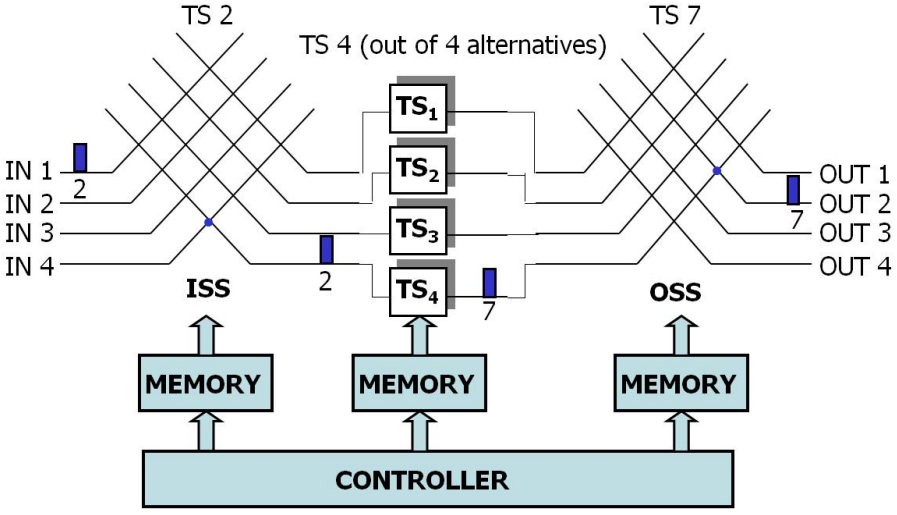
ST switch – 4 IN, 4 OUT – 120 chanels



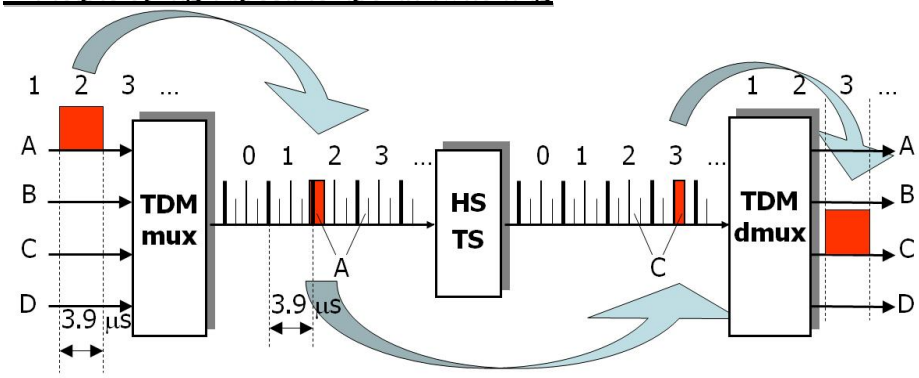
TST switch – 4 IN, 4 OUT – 120 channels



STS switch – 4 IN, 4 OUT – 120 channels



Principle of high speed temporal switching



4 x 2.048 Mb/s = 8.192 Mb/s

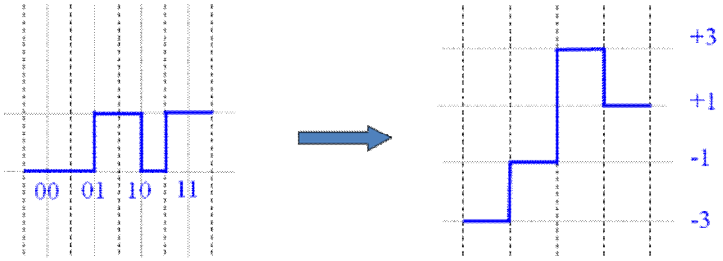
5. *Modulation techniques in DSL – list the techniques with full name and explain the principle of one of them*

https://intranet.etc.upt.ro/~DIG_INT_NET/course/5_Digital_subscriber_line_xDSL.pdf, 6-14

DSL Basics

- The most common DSL technologies are: IDSL, HDSL, SDSL, SHDSL, HDSL2, HDSL4, ADSL, RADSL, ADSL.lite, ADSL2, ADSL2+ and VDSL
- The emergence of DSL technologies allowed the development of new solutions for the redesign of the subscriber loop
- The modulations used in DSL are QAM, 2B1Q, DMT and CAP

2B1Q

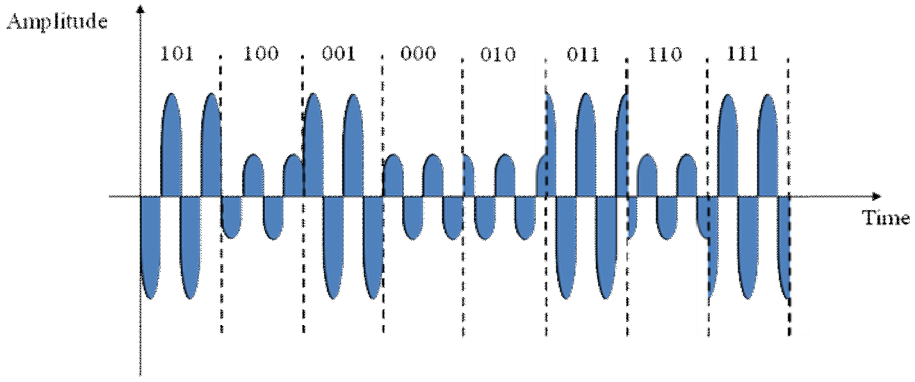


- The 2B1Q (*Two-Binary One-Quaternary*) line code was introduced together with the ISDN standardization, nowadays being used in HDSL, IDSL and SDSL technologies.

QAM

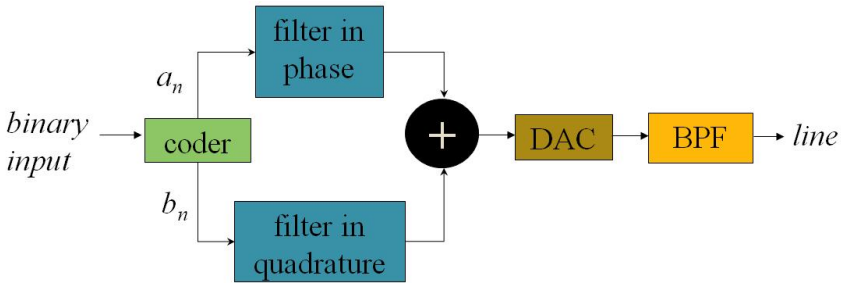
- QAM (*Quadrature Amplitude Modulation)* is a hybrid modulation
- The signal resulted at the output of the QAM modulator has the following expression:

$$s(t) = A\sqrt{\frac{2}{E_g}}g_T(t)\cos(2\pi f_c t + \theta)$$



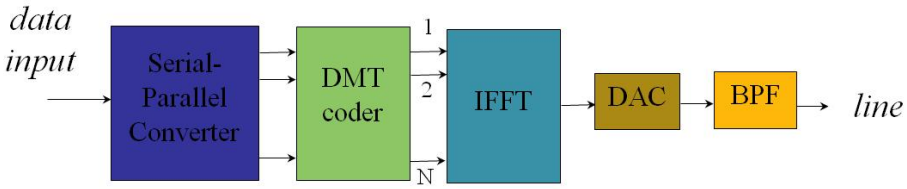
CAP

- CAP (*Carrierless Amplitude-modulation and Phase-modulation*) is a modulation technique derived from QAM, being, however, more easy to implement
- CAP modulation is used in SDSL, HDSL and ADSL technologies

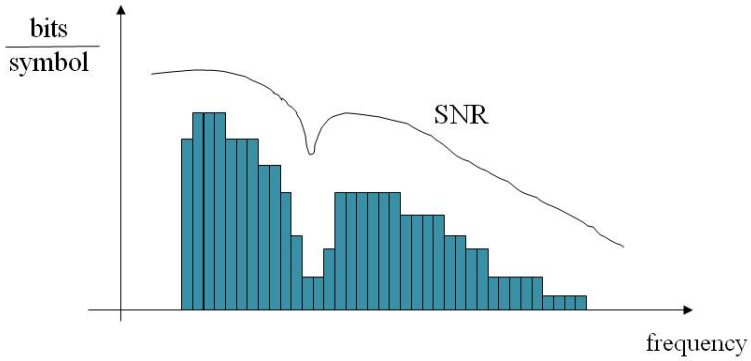


DMT

- DMT (Discrete multi-tone modulation) enables a subchannel division in a single modem



- DMT is a flexible modulation, mainly because of the bits distribution in the subchannel symbols



- According to ANSI, the DMT modulation can theoretically contain up to 255 subchannels centered on m·f frequencies where m = 1 ÷ 255 and f = 4.3125 kHz.
- DMT modulation is used in VDSL and ADSL technologies

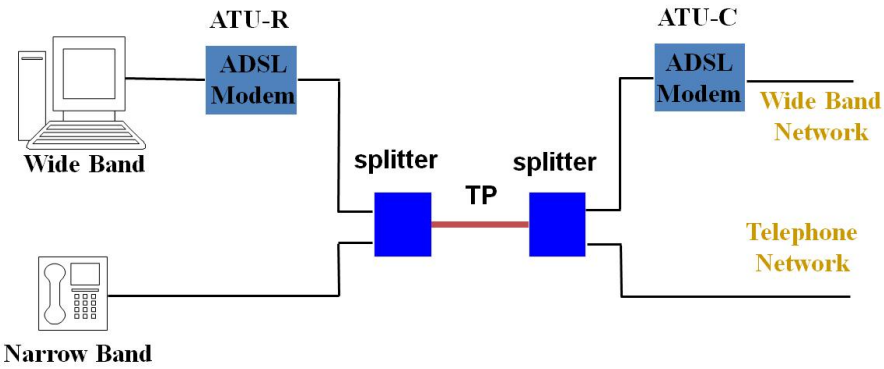
6. *ADSL – purpose, characteristics, basic schematic, frequency spectrum*

https://intranet.etc.upt.ro/~DIG_INT_NET/course/5_Digital_subscriber_line_xDSL.pdf, 35, 36, 38

ADSL - Asymmetric Digital Subscriber Line

- It represents a standard for digital communications, whose purpose is the high rate transmission of data over the telephone lines
- This technology was developed in 1989 at Bellcore Labs in order to provide video capabilities over standard telephone lines

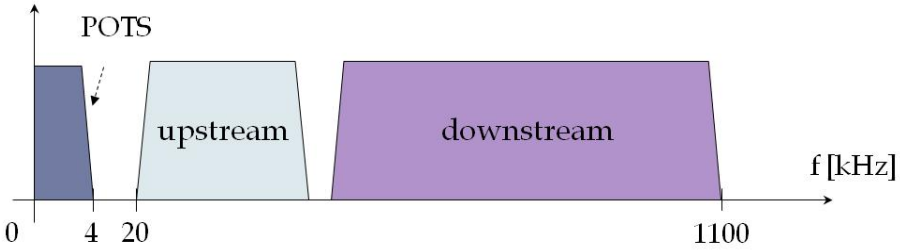
ADSL – basic schematic



ADSL – frequency spectrum

ADSL :

- system with FDM (*frequency division multiplexing*)
- available bandwidth for a single copper loop
- divided in 3 bands



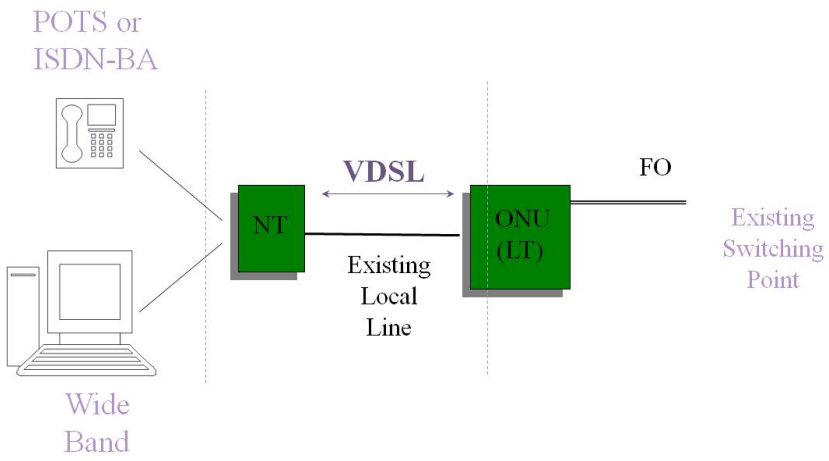
7. *VDSL – characteristics, the reference model for the interface, frequency spectrum and data rates*

https://intranet.etc.upt.ro/~DIG_INT_NET/course/5_Digital_subscriber_line_xDSL.pdf, 54, 56, 60, 62

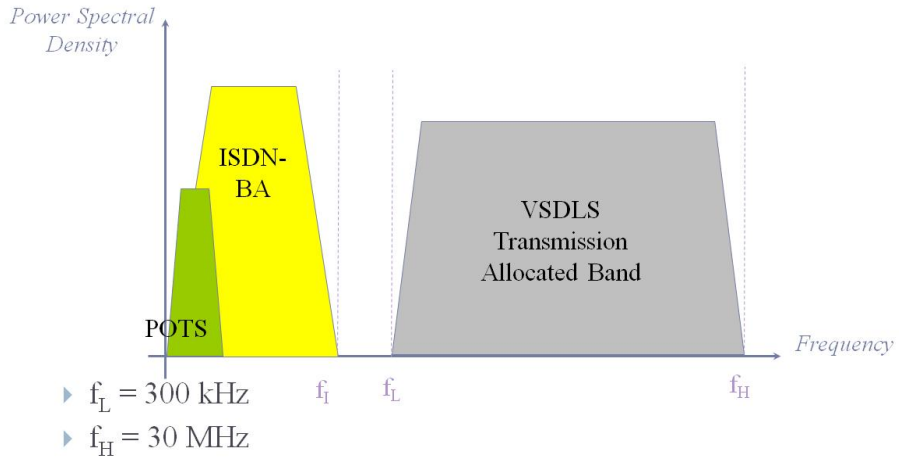
VDSL

- Very high bit rate Digital Subscriber Line
  - the DSL technology with the highest transmission rate
  - data rates
    - symmetric
    - asymmetric
    - up to tens of Mbps

VDSL – general architecture



VDSL – frequency spectrum



- $f_L = 300$ kHz
- $f_H = 30$ MHz

VDSL – bit rates

	Class of Operation	Downstream (kbps)	Upstream (kbps)
ASYM	Class I (A4)	362 x 64 = 23 168	64 x 64 = 4 096
	Class I (A3)	226 x 64 = 14 464	48 x 64 = 3 072
	Class I (A2)	134 x 64 = 8 576	32 x 64 = 2 048
	Class I (A1)	100 x 64 = 6 400	32 x 64 = 2 048
SYM	Class II (S5)	442 x 64 = 28 288	442 x 64 = 28 288
	Class II (S4)	362 x 64 = 23 168	362 x 64 = 23 168
	Class II (S3)	226 x 64 = 14 464	226 x 64 = 14 464
	Class II (S2)	134 x 64 = 8 576	134 x 64 = 8 576
	Class II (S1)	100 x 64 = 6 400	100 x 64 = 6 400

8. *Enumerate and explain the ISDN conditions*

https://intranet.etc.upt.ro/~DIG_INT_NET/course/6_ISDN.pdf, 1, 4, 6, 7

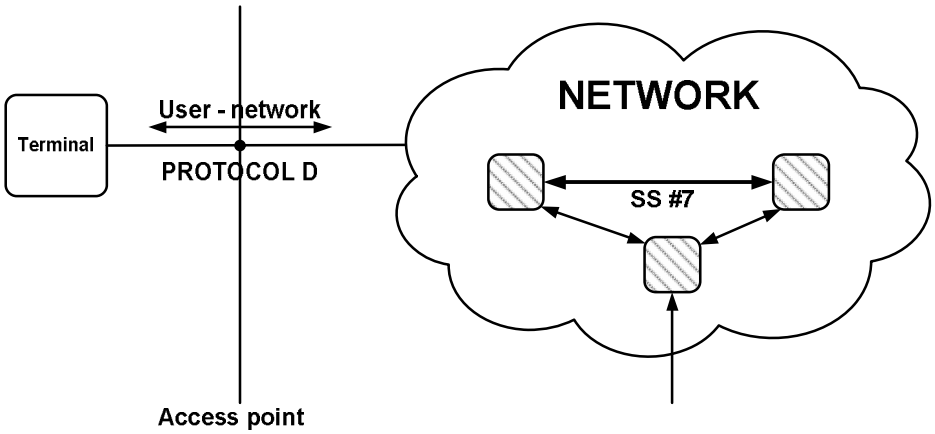
Integrated Services Digital Network

I.S.D.N. – *Integrated Services Digital Network*

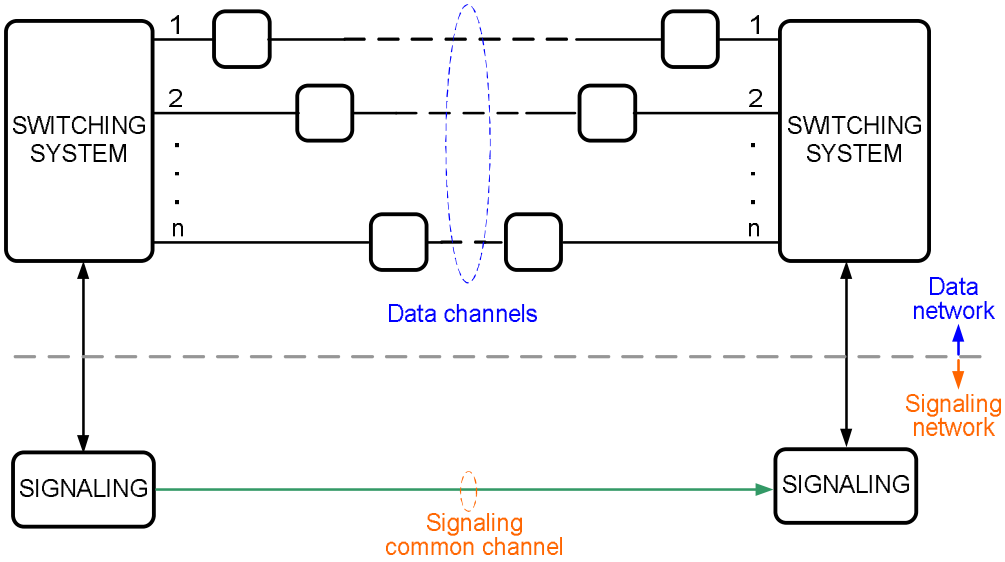
CONDITIONS

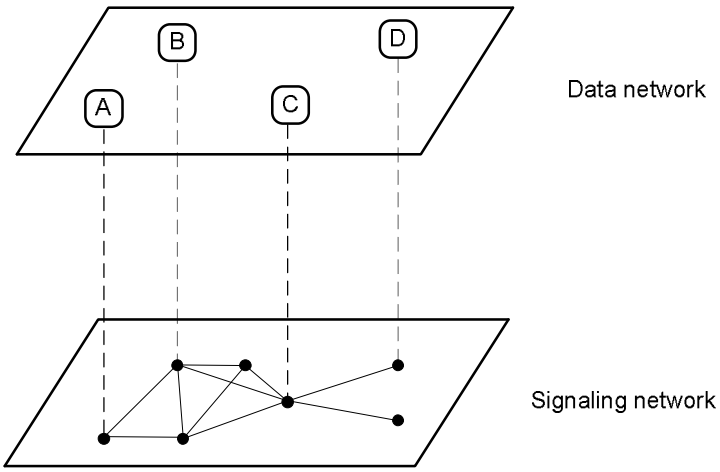
1. Digital connections from **terminal to terminal**
   - digital signal
   - digital subscriber line - DSL
   - digital transmission
   - digital switching
2. **Common-channel** signaling
3. **Multiple** network **access** for a wide range of voice and non-voice applications

Common channel signaling (I+III+IV)



Solution for intelligent network (ISDN)

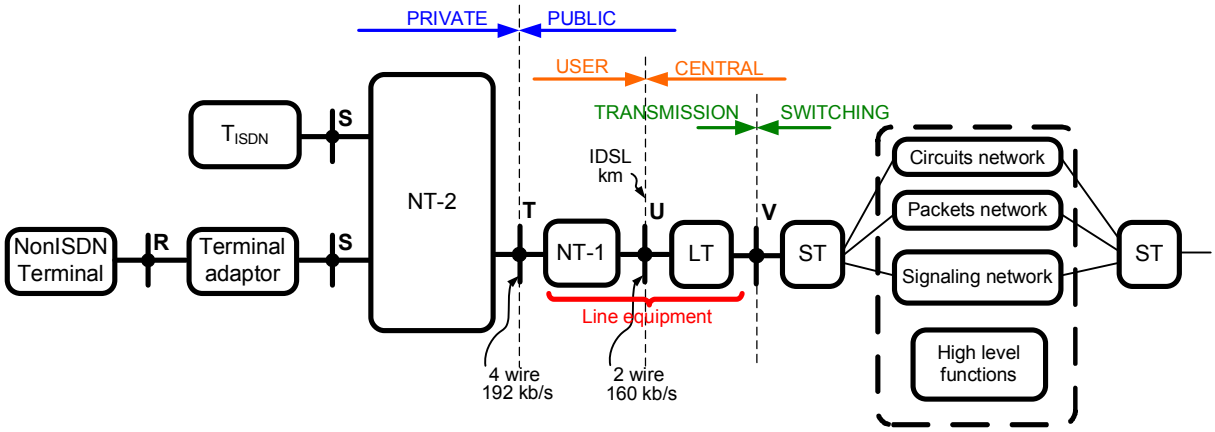




9. *Function groups and reference points – definitions, significances and domain limits.*

https://intranet.etc.upt.ro/~DIG_INT_NET/course/6_ISDN.pdf, 10

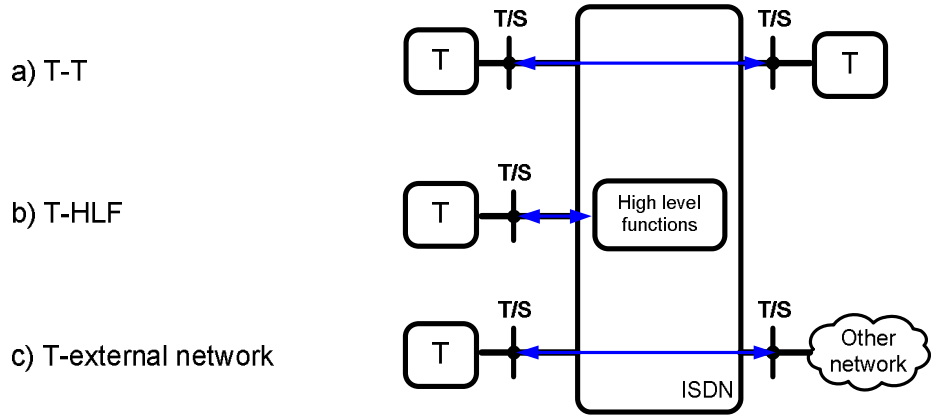
Function groups and reference points



10. Compare the bearer services with teleservices

https://intranet.etc.upt.ro/~DIG_INT_NET/course/6_ISDN.pdf, 11, 12

Intelligent network – bearer services



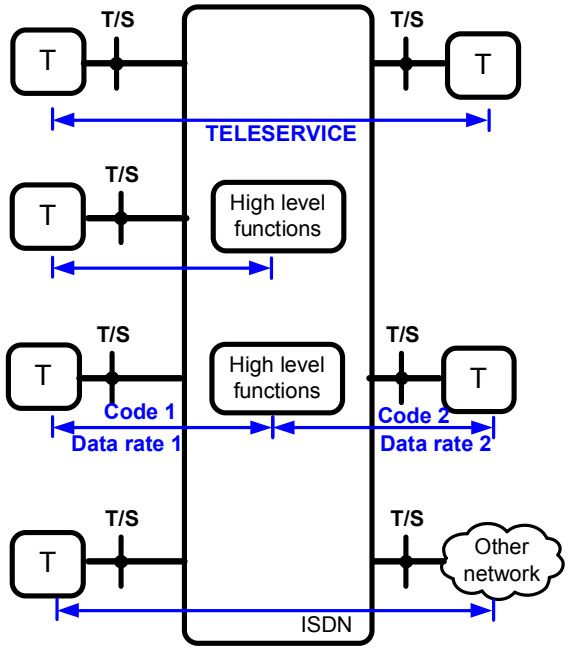
Intelligent network – teleservices

a) T-T

b) T - HLF

c) T-T using a HLF

d) T – specialized network



Data Communications

1. *Basic parameters of a communication system (power, bandwidth, signal to noise ratio)*

A: Course 1, slides 15,16,17.

Basic parameters of a communication system

- Transmitted power: the transmission power of the message signal [Watts]
- Frequency bandwidth: the physical spectrum available for a certain transmission [Hz, bps]
- Noises: undesired signals distorting the useful signal (channel noise, receiver noise, interferences)
- Shannon used these terms in its famous "capacity theorem"

Examples

- Bandwidth:
  - 300 – 3400 Hz for PSTN networks (adapted to the human hear's spectrum): restricted by regulations;
  - 1.1 MHz for twisted pairs cables (such as in PSTN): restricted by physical features;
  - 10 Mbps: total bandwidth available for an Ethernet transmission (100 Mbps for Fast Ethernet): restricted by regulations and physical features;

Power and noises

- SNR (signal-to-noise ratio):

$$SNR = \frac{P_{signal}}{P_{noise}} \qquad (1)$$

$$SNR[dB] = 10 \lg \frac{P_{signal}}{P_{noise}} \qquad (2)$$

- Examples: 0dB means unitary SNR, 10 dB means that the signal is ten times stronger, 20 dB means 100 times more signal power than noise power etc.

2. Write down the formula describing the Shannon capacity theorem for noisy channels, explain the meaning of each parameter and interpret the relation.

A: Course 2, slides 20, 21, 22.

THEOREM 2: *Let P be the average transmitter power, and suppose the noise is white thermal noise of power N in the band W. By sufficiently complicated encoding systems it is possible to transmit binary digits at a rate*

$$C = W \log_2 \frac{P+N}{N} \qquad (19)$$

with as small a frequency of errors as desired. It is not possible by any encoding method to send at a higher rate and have an arbitrarily low frequency of errors.

- This is the original Shannon formulation
- The widely used form is:

$$C = W \log_2 (1 + \frac{S}{N})$$

- For high values of SNR

$$C = \frac{W}{3} \frac{S}{N} [dB]$$

Signal to noise ratio

Interpretation: What Shannon says?

- Reminder: $C = W \log_2(1 + \frac{S}{N})$
- Capacity [bps], W[Hz]
- Shannon's formula expresses the theoretical maximum rate that can be achieved
- Shannon "decoded": Give me enough bandwidth, or enough power and we can shake the world !

The strength of Shannon's theorem lies in its degree of generality, while its complexity is low. Basically, Shannon states that the data rate at which information can be sent through a channel is limited by the bandwidth and by the signal to noise ratio (SNR). By its formulation, Shannon defined a theoretical capacity bound that describes the maximum theoretical bit rate which can be achieved through a channel with certain characteristics. This bound is taken as a reference point, and, for example, the performance of an error correcting code is largely evaluated by comparing the experimental BER with the a theoretical error probability issued from Shannon's law. Notice that, according to this theorem, the main resource of a communication system (that can increase the capacity) is the bandwidth W: if the bandwidth increase N times, the same happens with the capacity. Another valuable resource is the signal power, S, but the capacity increase with respect to S is only logarithmic.

Other remarks

- Only thermal noise taken into account in Shannon's formula
- Crucial effect: if R<=C, transmission can be performed without errors
- This capacity is called error-free capacity
- Example: telephone line with SNR=1000:1 (30 dB), C=30894bps

Notice that Shannon's capacity formula takes into account only the presence of the thermal noise, generally modeled as white Gaussian noise. Although most of the information theory relies on this assumption, in practice we oftentimes meet other types of noises that perturb the useful signal. If Shannon's formula still draw a maximal capacity curve, in the case where the signal is perturbed by other noises than the thermal noise, the performance of the system is further reduced.

3. Give the expression of the power spectral density of a thermal noise, indicating the meaning of each parameter.

A: Course 2, slide 11.

- Thermal noise
  - Generated by the thermal agitation of electrons
  - Uniformly distributed in frequency
  - Generally modeled as white noise
- The amount of thermal noise in 1Hz

$$N_0 = kT \qquad k = 1.3803 \cdot 10^{-23} \quad [J/^\circ K]$$

N_0 is the power spectral density [Watts/Hz]

- The amount of thermal noise in W Hz

$$N = kTW$$

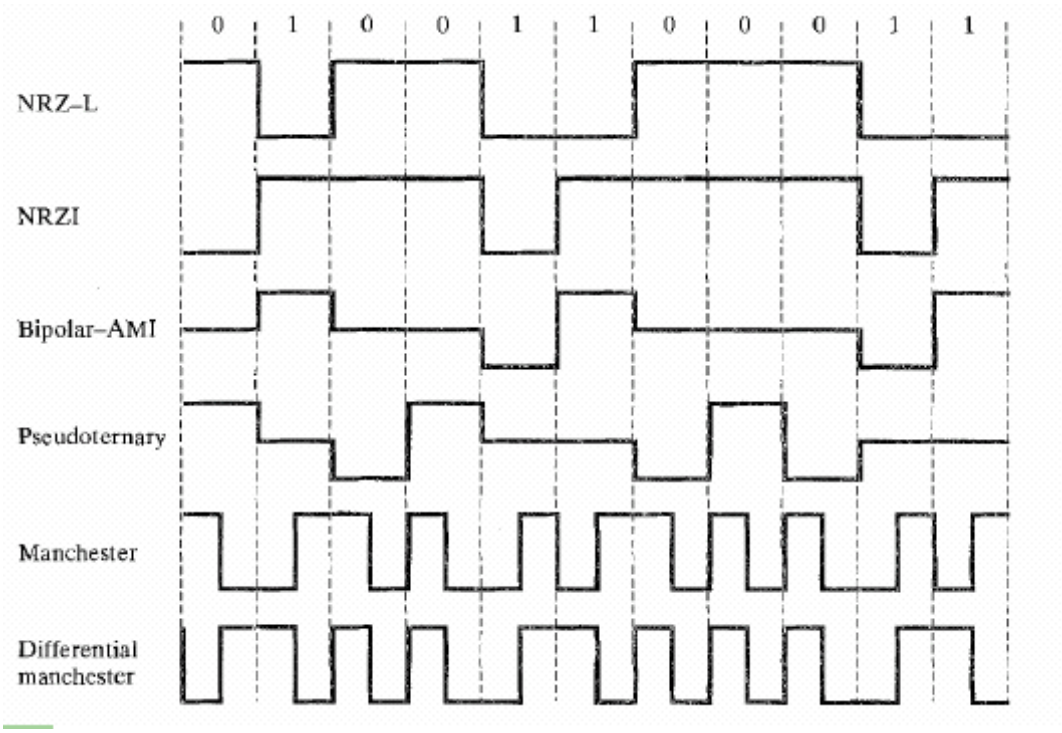
The thermal noise is present in all electronic circuits and transmission media. Generally, it is mathematically described as a "white noise". i.e. a noise whose power is uniformly distributed over the whole frequency bandwidth. This is the most common type of noise considered when modeling systems, and there is a huge amount of literature (information theory, coding, data transmission) built on the hypothesis that the noise that affects the signal is a white noise.

The power spectral density (PSD) of a white noise is constant and equals $N_0/2$ (if the representation considers the negative part of the frequency axis too), where N_0 depends on the temperature.

Notice that, larger the bandwidth, larger will be the amount of thermal noise "seen" by the receiver. We may therefore say that larger bandwidth transmissions are more affected by the thermal noise, compared to the narrower bandwidth transmissions.

4. Encode the bit sequence {0 1 0 0 1 1 0 0 0 1 1} using the following digital encoding techniques (NRZ-L, Binary AMI, Manchester and Manchester differential). Draw the encoded signal (Voltage levels are +A and -A).

A: Course 3, slide 26.



5.Encode the bit sequence {1100000110000000011} using the following scrambling techniques (B8ZS if the last non zero voltage was "-" and HDB3 assuming that since the last assuming that since the last substitution it was an odd number of 1's and the polarity of the preceding pulse was "-".). Draw the encoded signal (Voltage levels are +A and -A).

A: Course 3, slides pp.22, 23 and 29

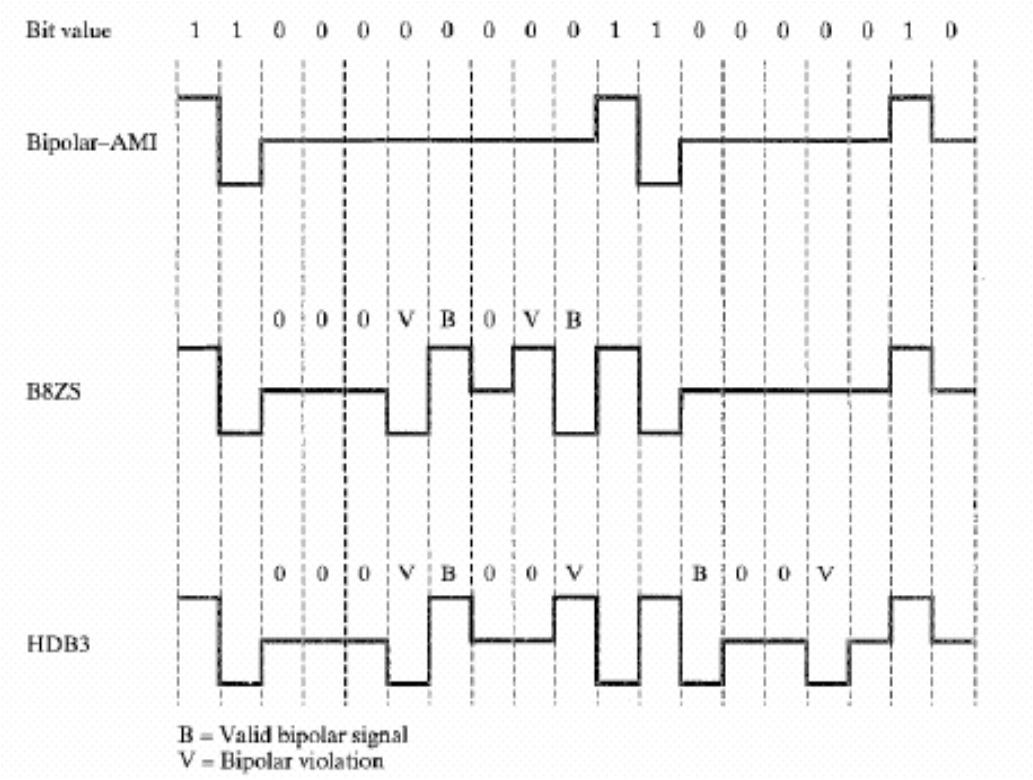
B8ZS

- Bipolar With 8 Zeros Substitution
- Can be considered as an improvement of the bipolar-AMI
- Rule: 8 consecutive zeros are NOT encoded with no signal for eight bit periods, a signal which has 4 transitions being used instead
- Whenever an all-zero octet occurs:
  - encode as 000+-0-+ if last non-zero voltage pulse was positive
  - encode as 000-+0+- if the last non zero pulse was a "-"
- AMI code rules are broken twice by "polarity violation": once inside of the eight-zeros group, once between the first non-zero pulse preceding the group and its correspondent within the group
- Unlikely to occur as a result of noise
- Receiver detects and interprets as octet of all zeros

HDB3

- High-density Bipolar, order 3
- Another improvement of the bipolar-AMI
- Rule: 4 consecutive zeros are NOT encoded with no signal for four bit periods, but with a signal which has at least one transition
- When a group of 4 zeros occurs:
  - encode as 000V if the number of bits of "1" after the last polarity violation is odd
  - B00V if the number of bits of "1" after the last polarity violation is even
  - V means the same polarity as the previous one, B respects AMI pattern
- This rule targets the elimination of the DC component (the polarity violation always changes its sign)

Both B8ZS and HDB-3 may be seen as improved versions of AMI. They are generally used in long-distance communications. The scrambling techniques have some basic error detection capabilities. E.g.: when in HDB3 two consecutive polarity violations have the same sign, this could be only caused by a transmission error.



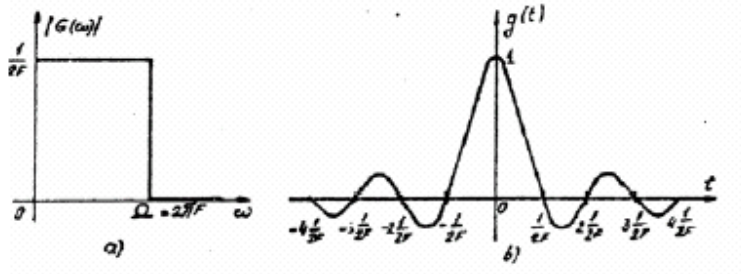
6. Give the expression of the Nyquist rate for ISI-less transmission, indicating the meaning of each term.

Course 4, slides 10, 11.

Nyquist theorem

- In a channel which is equivalent with an ideal low-pass filter having the cutoff frequency F, it is possible to transmit symbols with a modulation rate equal or less to 2F symbols/sec, without ISI
- The characteristics of such a channel are shown below

Transfer function | Impulse response



According to the Nyquist theorem, the best spectral efficiency for an ISI-less data transmission (that is the highest ratio between R (rate) and W (bandwidth)) can be achieved if every symbol is shaped as a cardinal sine, which corresponds to an ideal LPF. In this case only, the transmission can be made at a symbol rate which is twice the bandwidth, while preserving it free of ISI. That's why this transmission rate is sometimes referred to as "ideal rate" or "Nyquist rate".

Ideal case: a closer look

- The impulse response of the ideal low-pass filter is:

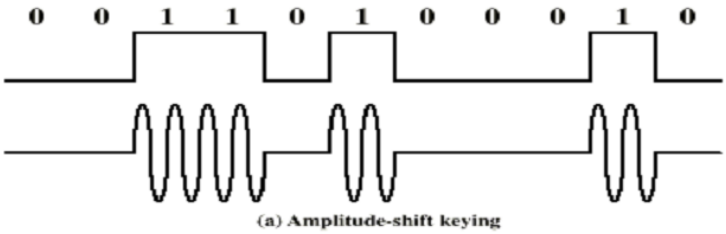
$$g(t) = \frac{\sin(\Omega t)}{\pi t} = \frac{\sin\frac{2\pi}{T_0}t}{\pi t} \quad (11)$$

- Such a waveform crosses zero every $T_0/2$ seconds
- In frequency, this corresponds to an ideal low-pass (brick-wall) filter, with the cut-off frequency $F=1/T_0$
- If a symbol is issued every $T_0/2$ seconds, transmission can be made without ISI
- The rate in this case will be 2F symbols/s (Nyquist rate, ideal rate)

Although, unlike in the digital baseband transmission (e.g.:NRZ), a single information symbol is represented by a waveform with infinite duration (a cardinal sine), we can transmit the next information symbol at the first zero crossing of the sinc waveform (i.e.: at $T_0/2$); this will prevent ISI to occur and will allow a transmission at a rate of $2/T_0$ symbols/sec. The later statement is identical with Nyquist's theorem, formulated on the previous slide.

7. Give one graphical example illustrating a signal obtained by digital AM. A: Course 5, page 3, first slide.

- AM is referred to as linear modulation
- The amplitude of the carrier is changed by the signal to be transmitted
- When the modulating signal is digital, the Amplitude Shift Keying (ASK) case is obtained
- The simplest form of ASK is called On/Off Keying (OOK)



(a) Amplitude-shift keying

8. *What do the following terms mean: DSB-AM, SSB-AM, VSB-AM?*

A: Course 5, slides from pp. 5-7.

Suppressing…and un-suppressing the carrier

- If the carrier has a DC component:

$$c(t) = c_0 + \cos(\omega_0 t + \varphi_0) \quad (2)$$

- The modulated signal is:

$$s_a(t) = (s(t) + c_0)\cos(\omega_0 t + \phi_0) \quad (3)$$

- In the spectrum, we will retrieve the Dirac pulses corresponding to the sine carrier

$$S(\omega) = H(\omega)\left\{\pi c_0[\delta(\omega+\omega_0)+\delta(\omega-\omega_0)]+\left[\frac{1}{2}G(\omega+\omega_0)+\frac{1}{2}G(\omega-\omega_0)\right]\right\} \quad (4)$$

Remarks

- If c_0=0, then we have AM with suppressed carrier
  - The figures from the next slide correspond to the above case
- The later is also called product modulation, because it consists on a simple multiplication
- All the information of the AM signal is carried by EACH side-band
- From effectiveness reasons, one side-band can be suppressed

Graphical illustration

- The filter selects the lower (inferior) or the upper (superior) side-band, leading to Single Side Band (SSB) AM

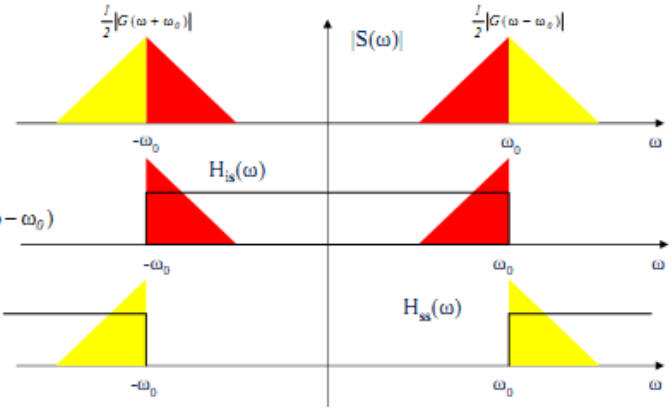
a. Double side-band AM

b. Inferior SB AM

$H_{IS}(\omega) = \sigma(\omega+\omega_0) - \sigma(\omega-\omega_0)$

c. Superior SB AM

$H_{ss}(\omega) = 1 - H_{IS}(\omega)$



SSB-AM

- SSB signal can be expressed as:

$$s_{si}(t) = \frac{1}{2} g(t)\cos(\omega_0 t) + \frac{1}{2}\hat{h}\{g(t)\}\sin(\omega_0 t) \quad (5)$$

- $\hat{h}\{g(t)\}$ is the Hilbert transform of g, which can be obtain by passing g(t) through the filter:

$$F(\omega) = -j\,\mathrm{sgn}(\omega) \quad (6)$$

- SSB-AM is spectrally efficient
- Difficult to implement in practice: the filters which separate the side-band must be very selective

AM with Vestigial Side-Band (VSB)

- Only part of the side-bands is suppressed
- Lower frequencies transmitted with both Side-Bands, upper frequencies with one side-band
- This allows easier filtering to separate the bands (frequencies near the carrier must not be filtered)
- 25% more bandwidth required than in SSB, but easier to implement
- Example: NTSC TV system: all upper sideband of bandwidth W2 = 4 MHz, but only W1 = 1.25 MHz of the lower sideband are transmitted

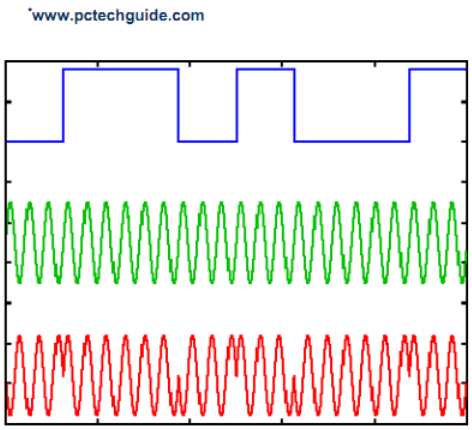
AM signals demodulation

- AM modulation with suppressed carrier is discussed
- Two types of detection for AM: coherent and non-coherent
- Even if simpler, the non-coherent detection is very sensitive to noise
- Coherent detection is oftentimes preferred

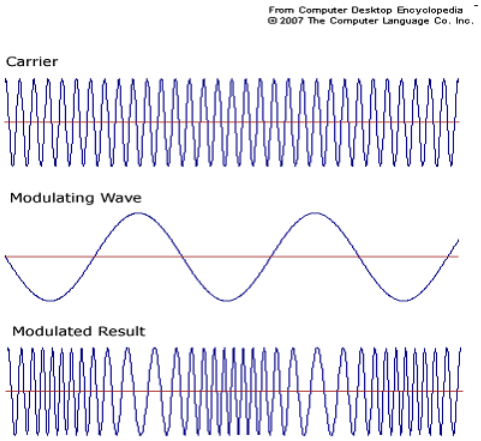
9. Explain the meaning of the term PSK and represent graphically a PSK signal.

A: Course 7, slides 4-5.

- Definition: PM is a method used to transmit analog or digital signals, in which the information is carried by the initial phase of a high-frequency carrier
- PM is not so popular as FM, especially for analog signal modulators (because of its complexity)
- When the modulator is digital, the frequency modulation is referred to as phase shift keying (PSK)



PSK



Analog PM

10. Write down the expression that describes the orthogonality of the OFDM carriers. What is the relation between the OFDM symbol duration (T) and the fundamental frequency (f0)? A: Course 11, slide 10.

Orthogonal carriers

- The OFDM carriers are orthogonal, their frequencies being f_0, $2f_0$, $3f_0$ etc.

$$\frac{2}{T}\int_{kT}^{(k+1)T} \sin(mf_0t)\cdot\sin(nf_0t)\cdot dt = \begin{cases} 1, \text{ if } m=n \\ 0, \text{ if } m\neq n \end{cases} \quad (1)$$

- Complex exponentials of limited duration used in practice
  - Their duration equals OFDM's symbol time (T)
- The orthogonality is met if: $f_0=1/T$

Audio and Video Systems

1. *Digitization parameters and data rates for voice and hi-fi audio*

https://intranet.etc.upt.ro/~AVS/Course/1_MULTIMEDIA.PDF, 15,16

- **High-quality stereo standard**
  - CD standard, hi-fi music, 20 kHz audio bandwidth
  - 2 channels
    - for **stereo** recording and transmission
  - f_E = 44.1 kHz
    - **sampling rate**, according to Shannon's theorem
  - n = 16 bits
    - for **quantization** with SNR = 96 dB

  ⇨ data rate: 2 × 44.100 × 16 = 1 411 200 bits/s

- **Speech-quality standard**
  - telephony standard, voice, 3,4 kHz audio bandwidth
  - 1 channel
    - for voice **recognition**
  - f_E = 8 kHz
    - **sampling rate**, according to Shannon's theorem
  - n = 8 bits
    - for **quantization** with SNR = 48 dB

  ⇨ data rate: 1 × 8.000 × 8 = 64.000 bps

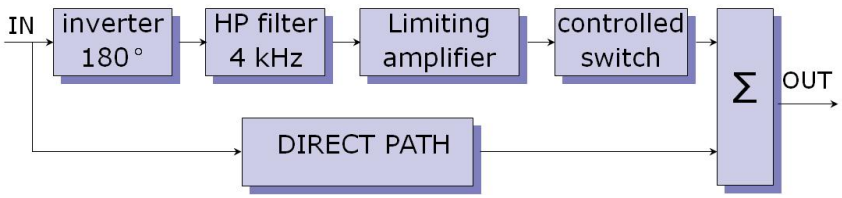
2. *Noise reduction principles*

https://intranet.etc.upt.ro/~AVS/Course/2_SOUND.PDF, 23-28

Playback noise reduction (I+II)

- **NOISE** ⇔ signal with low level and middle to high **frequency**

  ⇨ such a signal can be identified and **rejected** (noise gate)
- **Example**: Philips **DNL** (*Dynamic Noise Limiter*)



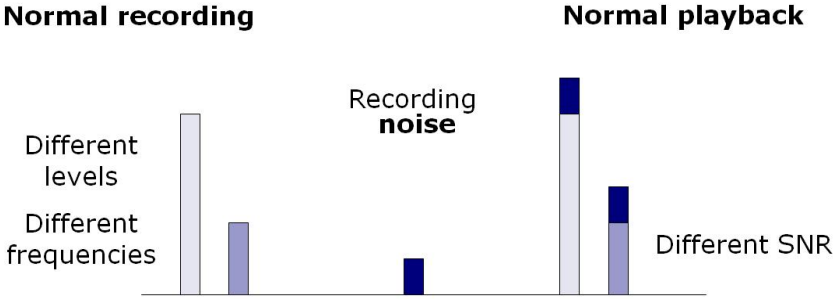
IN: signal with noise

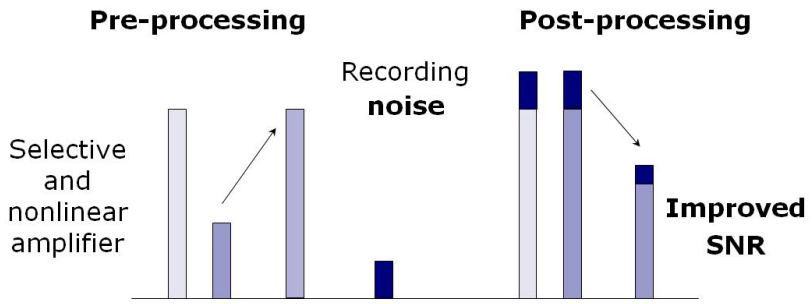
OUT: signal with **improved SNR** with **8 dB**

- **DNL advantage**:
  - works with any recording system on **any playback system**
- **How DNL works in different situations:**
  - during the **pause** between melodies
  - high level recorded music
  - low level recorded music
- **DNL disadvantage**:
  - it cannot make the difference between noise and the real signal

Recording & playback noise reduction systems (I+II)

- The systems perform:
  - signal processing before recording
  - opposite processing after playing back





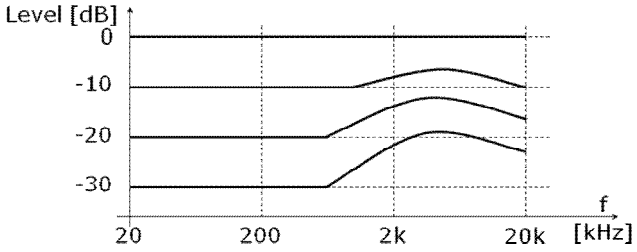
Advantage:

- the real signal is **not altered** and obtained with a **high SNR**

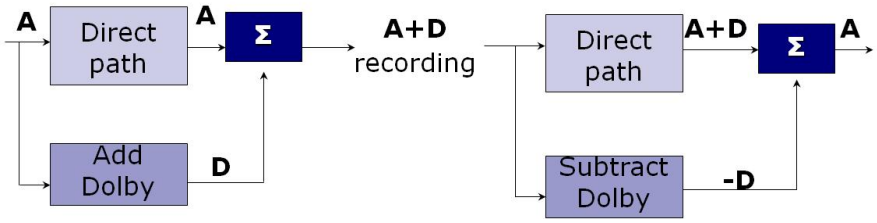
Disadvantage:

- it only works on the same system (record and playback)

Dolby system (I+II)



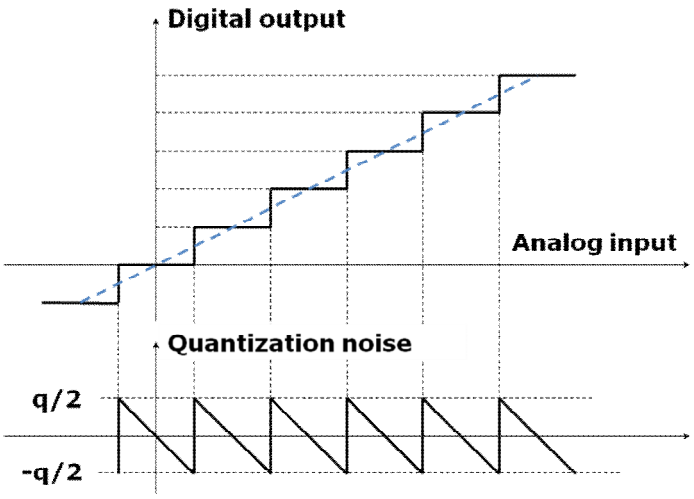
- **NOISE**:
  - high frequency (1 ÷ 15 kHz)
  - low level (-20 ÷ -40 dB)
- **DOLBY** circuits:
  - amplify **nonlinearly** and **selectively** when recording
  - performs opposite processing on playing the signal
  - **Increases SNR** with 9 dB

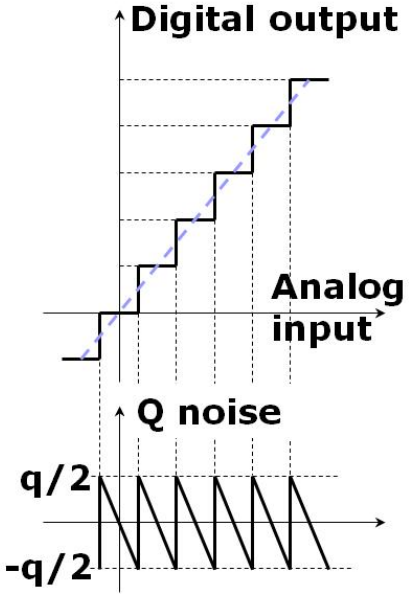


3. Quantization techniques

https://intranet.etc.upt.ro/~AVS/Course/2_SOUND.PDF, 36, 37, 41, 42

Uniform quantization (I+II)





- **decision levels** (analog input)
  - ☐ **uniform**
- **quantization levels** (digital output)
  - ☐ **uniform**
- **quantization steps** (q) are **constant:**
  - ☐ for low level signal
  - ☐ for high level signal
- **quantization noise** (error): -q/2 ÷ q/2

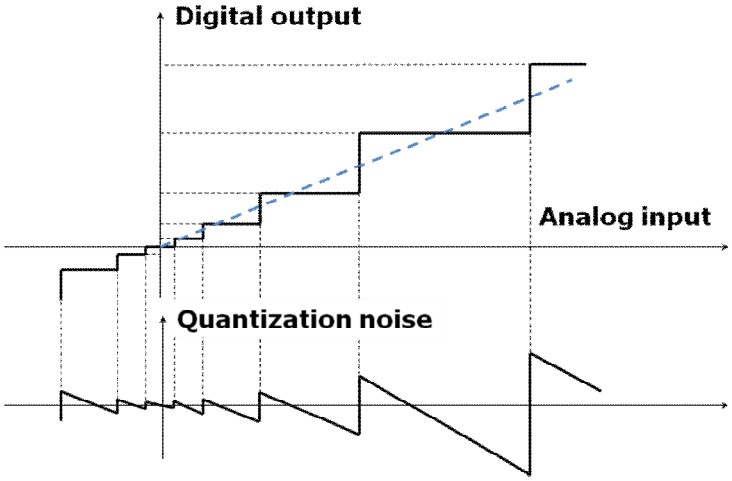
RESULT

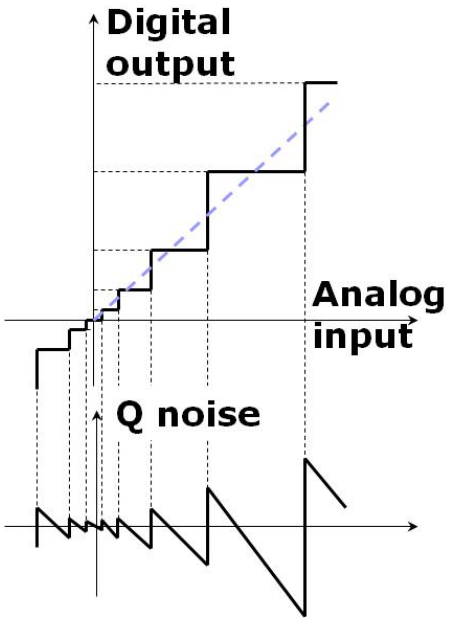
- **low level signal with** constant quantization error ⇨ **low SNR**
- **high level signal with** constant quantization error ⇨ **high SNR**

CONCLUSION

- **low general SNR (⇔ low quality)**

Non-uniform quantization (I+II)





- **decision levels** (analog input)
  - **non-uniform**
- **quantization levels** (digital output)
  - **non-uniform**
- **quantization steps** (q) are **different:**
  - for low level signal
  - for high level signal
- **quantization noise** (error):
  - **non-constant**

RESULT

- **low level signal with** low quantization error ⇨ **high SNR**
- **high level signal with** high quantization error ⇨ **high SNR**

CONCLUSION

- **high general SNR (⇔ high quality)**

4. The digital photo camera – adjustments, structure

https://intranet.etc.upt.ro/~AVS/Course/3_EC_image_web.pdf, 6-9

Photographic image acquisition (II)

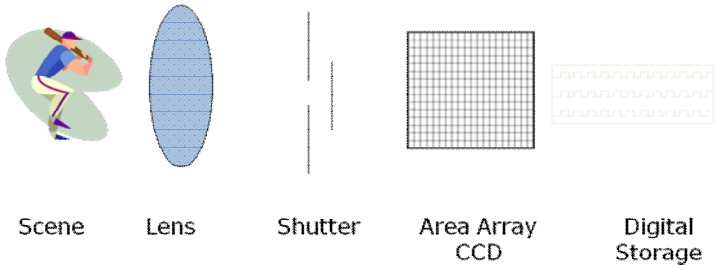
- **Conventional** image **capture** needs the following main components:
  - LENS
    - to **focus the light** from a scene onto a photosensitive film (silver)
  - IRIS
    - to control the **amount of light** which hits the film
  - SHUTTER
    - to control the **timing** of the light exposure of the film

Electronic image acquisition (I+II)

- The **electronic** image is obtained using:
  - traditional elements: lens, iris, shutter
  - additional components:
    - **CCD** (Charge Coupled Device)
      - image **scanning** and **photo-electric** conversion
    - **ADC** (Analog to Digital Converter)

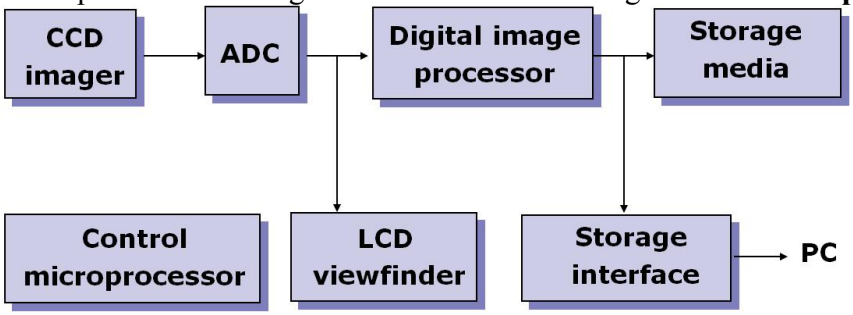
- delivering the **digital format** of the image

- **Digital storage media**
  - **electronic** memory, **magnetic** support (disk or tape), optical support



Digital photo camera (I)

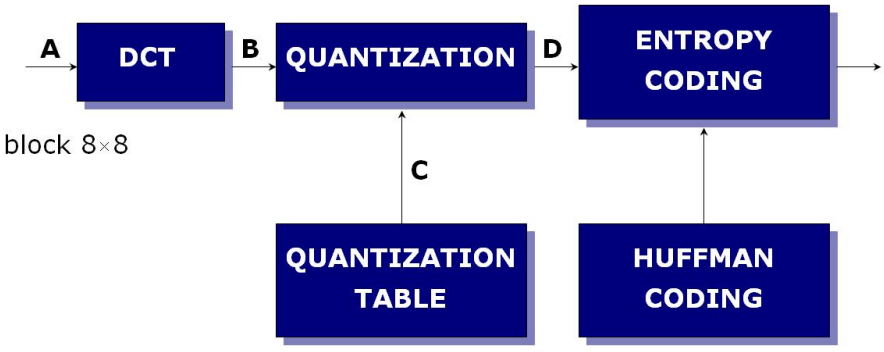
- A portable still image camera has the following **electronic components**:



5. The principle of JPEG compression

https://intranet.etc.upt.ro/~AVS/Course/3_EC_image_web.pdf, 62-66

JPEG Methodology (I+II+III)



- **DCT**
  - transforms **time** representation block **A**
    (lot of data points)

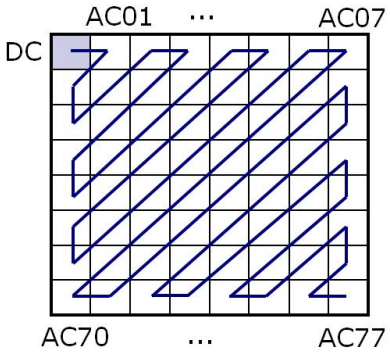
- in **frequency** representation block **B**
  (few data points – few frequency components)
- **QUANTIZATION**
  - reduces **non-uniformly** the accuracy of coefficients, **D**, according to the quantization table **C** (**4 tables** implemented in JPEG algorithm):
    - **low frequency** with higher accuracy
      (small steps, non-zero values)
    - **high frequency** with lower accuracy
      (big steps, most values equal to zero)
- **ENTROPY CODING**
  - is used to obtain **data compression**
  - zig-zag scanning is used to obtain **long sequences of "zero"**
    - **RLE** (Run-Length Encoding) - offers an excellent compression
    - **Huffman coding -** is used to obtain higher compression factor

Discrete Cosine Transform (I+II)

- **DCT** (similar to Fourier transform) converts data from
- from **time domain**
  - 8×8 pixels block:
    - rows 0 ÷ 7
    - columns 0 ÷ 7
- to **frequency domain**
  - 8×8 coefficient matrix
  - 00 position
    - DC coefficient
      - average of the 8×8 block
  - 01 ÷ 77 positions
    - AC coefficients
      - low frequency in the upper left corner
      - high frequency elsewhere

Zig-zag sequencing

- starts with low frequency coefficients (non-zero),
- then high frequency coefficients (zero);
- results a long sequence of zeros, after a few significant values, easy entropy coding (RLE, Huffman)

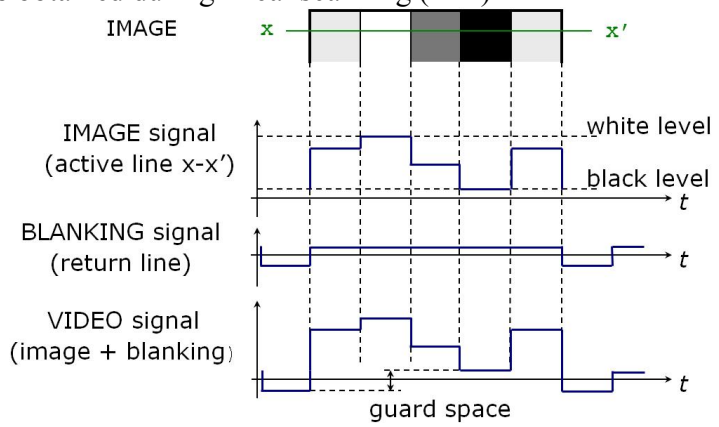


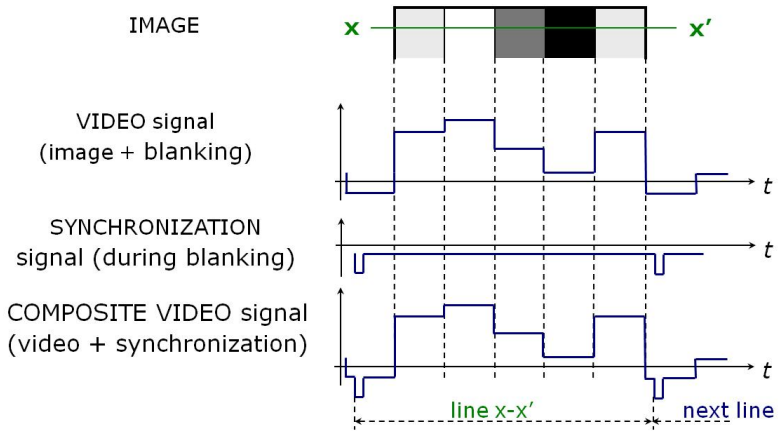
6. The composite video signal (components, parameters, TV line oscillogram)

https://intranet.etc.upt.ro/~AVS/Course/4.1_EC_TV_web.pdf, 9, 10, 12

Composite video signal (I+II)

Is obtained during linear scanning (x-x')





Frequency of composite video signal (II)

- Aspect ratio
  - 4 × 3
- Vertical resolution
  - 575 visible lines (out of 625)
- Horizontal resolution

  For best resolution perception, the pixel must be **square**
  - 4 / 3 × 575 = 766 pixels

7. Color TV signals

https://intranet.etc.upt.ro/~AVS/Course/4.1_EC_TV_web.pdf, 21-23

Color TV signals (I+II)

- Luminance of a (color) image is used in black-and-white television:

  Y = 0.3×R + 0.59×G + 0.11×B
- Using R, G, B signals would be incompatible with the old TV system.
- Compatible color TV systems use:
  - Y – **luminance**

    (for correct processing by black-and-white TV sets)
  - C – **chrominance**

    (color information only, no brightness information)

    ⇨ **color difference** signals: **R-Y, G-Y, B-Y**
- From the 4 signals, only 3 are used:
  - luminance
    - Y = 0.3×R + 0.59×G + 0.11×B
  - chrominance (2 color difference)
    - R-Y = 0.7×R – 0.59×G – 0.11×B
    - B-Y = -0.3×R – 0.59×G + 0.89×B

Compatible TV signals (I)

- **Luminance**

  $E_Y = 0.3 \times E_R + 0.59 \times E_G + 0.11 \times E_B = 0 \div 1$
- **Color difference**

  $E_{R-Y} = 0.7 \times E_R - 0.59 \times E_G - 0.11 \times E_B = -0.7 \div 0.7$

$E_{G-Y} = -0.3 \times E_R + 0.41 \times E_G - 0.11 \times E_B = -0.41 \div 0.41$ (not transmitted)

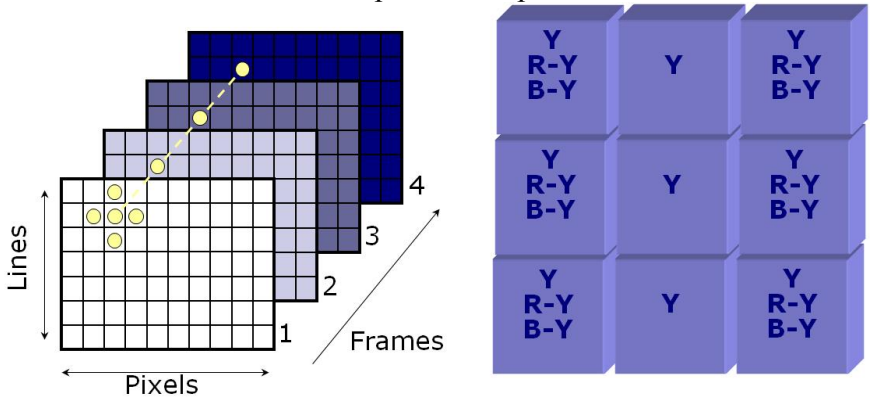
$E_{B-Y} = -0.3 \times E_R - 0.59 \times E_G + 0.89 \times E_B = -0.89 \div 0.89$

8.Digitization parameters, basic sampling formats and corresponding data rates for the TV signal

https://intranet.etc.upt.ro/~AVS/Course/4.5_E_DTV_web.pdf, 3-5, 12, 13

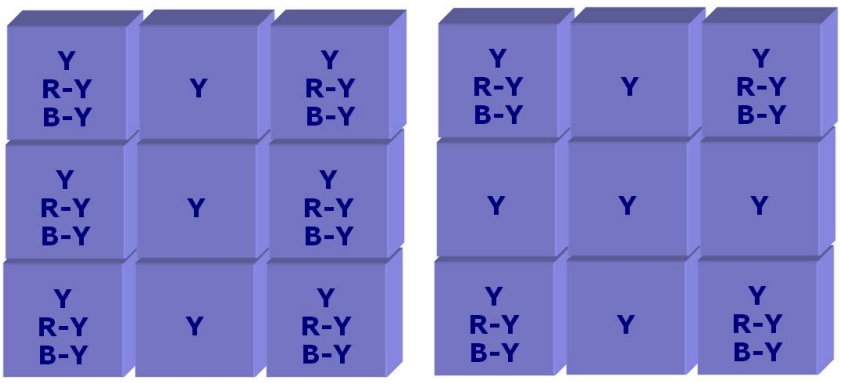
Digital TV studio standard (I+II+III)

- 1982, CCIR Rec.601 – **USA/Europe** standard
  - NTSC / SECAM / PAL
  - 525 / 625 lines
  - common **digital TV line**
    - same bit **rate**
    - same quality
    - easy system conversion
- TV components (**Y**, **R-Y**, **B-Y**)
  - **orthogonal** sampling
  - standard sampling frequency
    - f_S **= 13,5 MHz**
  - PCM format
    - **8 bits** / component sample



4:2:2 format

STUDIO quality



4:2:2 format
STUDIO quality

4:2:0 format
BROADCASTING quality

Digital television signal bit rate

- Digital signal bit rate
  - $D = f_S \times n$ [bits/s]
- TV signal bit rate
  - $D = D_Y + D_{R\text{-}Y} + D_{B\text{-}Y}$

    $= f_{S\,Y} \times n_Y + f_{S\,R\text{-}Y} \times n_{R\text{-}Y} + f_{S\,B\text{-}Y} \times n_{B\text{-}Y}$
- 4:2:2 format - TV signal bit rate
  - D_{TV} = 13.5 MHz × 8 b + 6.75 MHz × 8 b + 5.75 MHz × 8 b =

    = 108 Mbits/s + 54 Mbits/s + 54 Mbits/s = **216 Mbits/s**

Digital television standard family

	Standard	**Parameters**	D_Y	$D_{R\text{-}Y}+D_{B\text{-}Y}$	D [Mbps]
HIGHER ORDER FORMATS	4:4:4 progressive	f_H = 31.250 Hz f_S = 27 MHz	216	216+216	648
	4:4:4 interlaced	f_H = 15.625 Hz f_S = 13,5 MHz	108	108+108	324
BASIC FORMAT	4:2:2 studio	f_{SY} = 13,5 MHz f_{SC} = 6,75 MHz	108	54 + 54	216
LOWER ORDER	4:1:1	f_{SY} = 13,5 MHz f_{SC} = 3,375 MHz	108	27 + 27	162

FORMATS	4:2:0 broadcast	alternative on lines	4:2:2 4:0:0	108	54 + 54 0 + 0	162
	2:1:1	f_{SY} = 6,75 MHz f_{SC} = 3,375 MHz		54	27 + 27	108

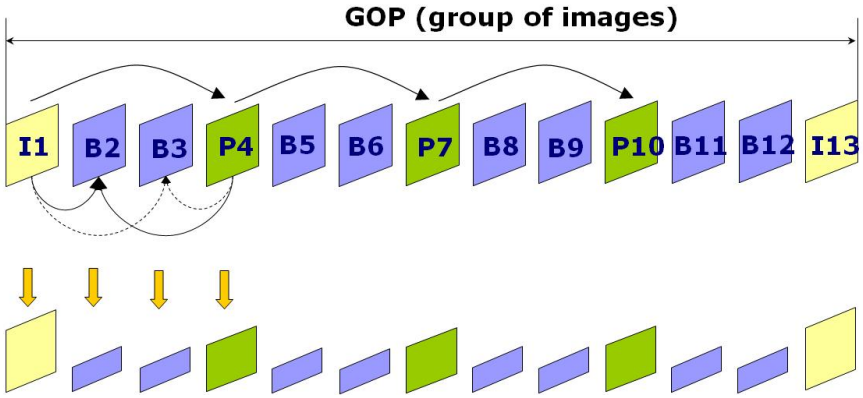
9. The principle of MPEG compression

https://intranet.etc.upt.ro/~AVS/Course/4.6_E_MPEG_web.pdf, 7-9

MPEG coding (I+II)

- **Spatial** redundancy removal
  - DCT
- **Temporal** redundancy removal
  - Motion-compensated forward
  - Bidirectional prediction (interpolation)
- MPEG uses three **types of images**
  - **Image I**
    - **JPEG** coded
    - independent to the sequence of moving images
    - **robust** coding
    - independent to precedent errors
    - **low** compression factor
  - **Image P**
    - a **predicted** image is estimated (motion-compensated forward)
    - the **difference** between actual and predicted image is **coded**
    - sequence of predictions may propagate possible **errors**
    - **higher** compression factor
  - **Image B**
    - a bidirectional **interpolated** image is calculated, using I and P images
    - very good estimation
    - may propagate **errors**
    - **best** compression factor

Moving pictures digital compression (I)



Compression

- Different techniques are used
- Resulting different factors

10. The structure and the parameters of a TV channel

https://intranet.etc.upt.ro/~AVS/Course/4.4_E_RF_web.pdf, 3, 5

Modulation methods

- Amplitude modulation
  - **AM**

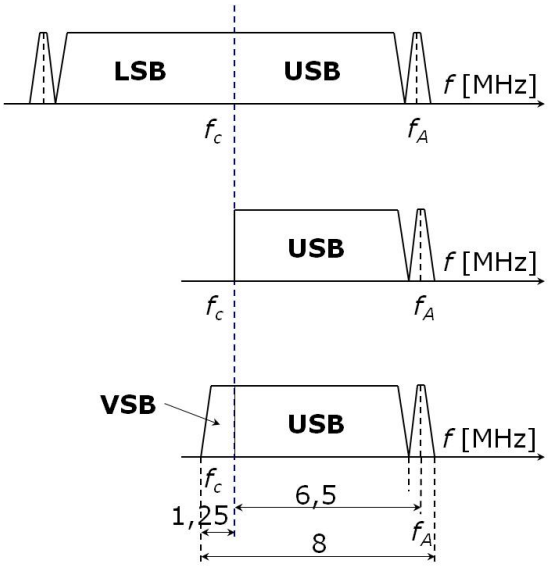
  ⇨low power efficiency

- Single Side Band AM
  - **SSB-AM**

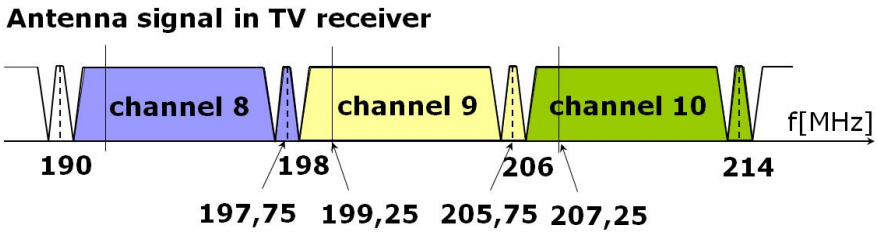
  ⇨impossible to filter

- Vestigial Side Band AM
  - **VSB-AM**

  ⇨standard solution



Intermediate frequency processing



A **single filter** for:

- channel **extraction**
- adjacent channel **rejection**
- **VSB** rejection